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PATENT RS

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7-14-03



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Branko Kovacevic et al.

Title: **METHOD FOR SYNCHRONIZING TO A DATA STREAM**

Application No.: 09/491,119

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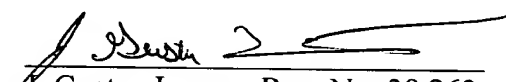
SUBMISSION OF NEW FORMAL DRAWINGS

Transmitted herewith are thirty-nine (39) sheets of new drawings containing Figs. 1-7, 8 & 9, 10-17, 18 & 19, 20-23, 24 & 25, 26-29, 30 & 31, 32-43, respectively.

Respectfully submitted,

7-7-03

Date

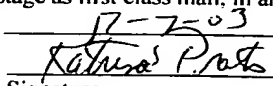

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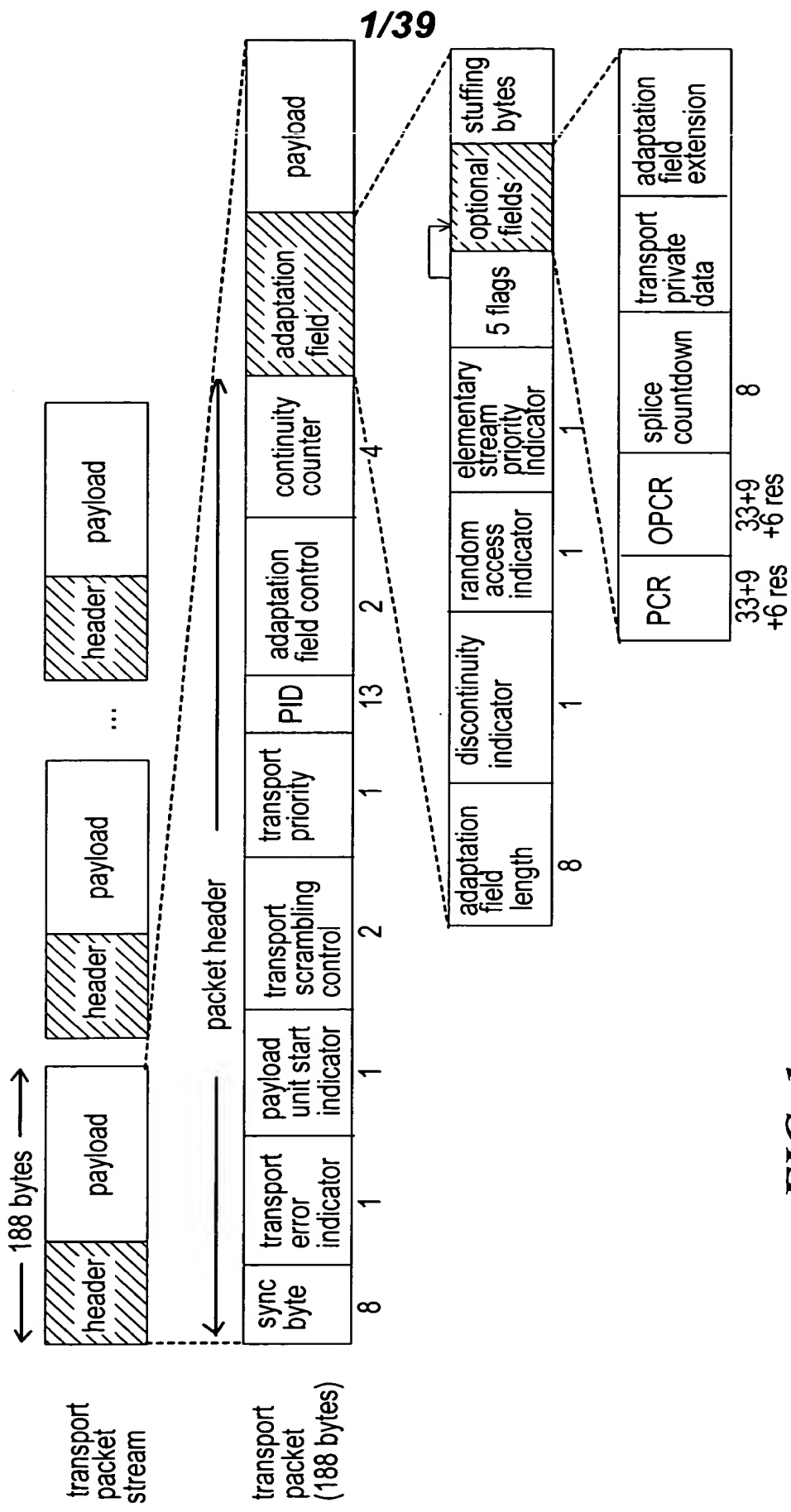


FIG. 1
--PRIOR ART--

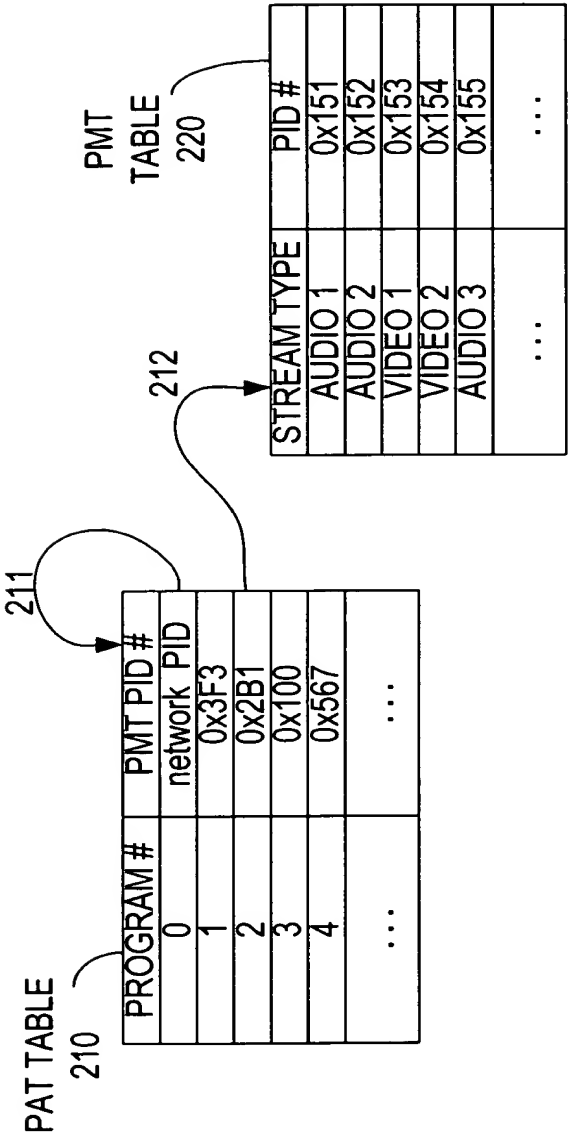


FIG. 2
--PRIOR ART--

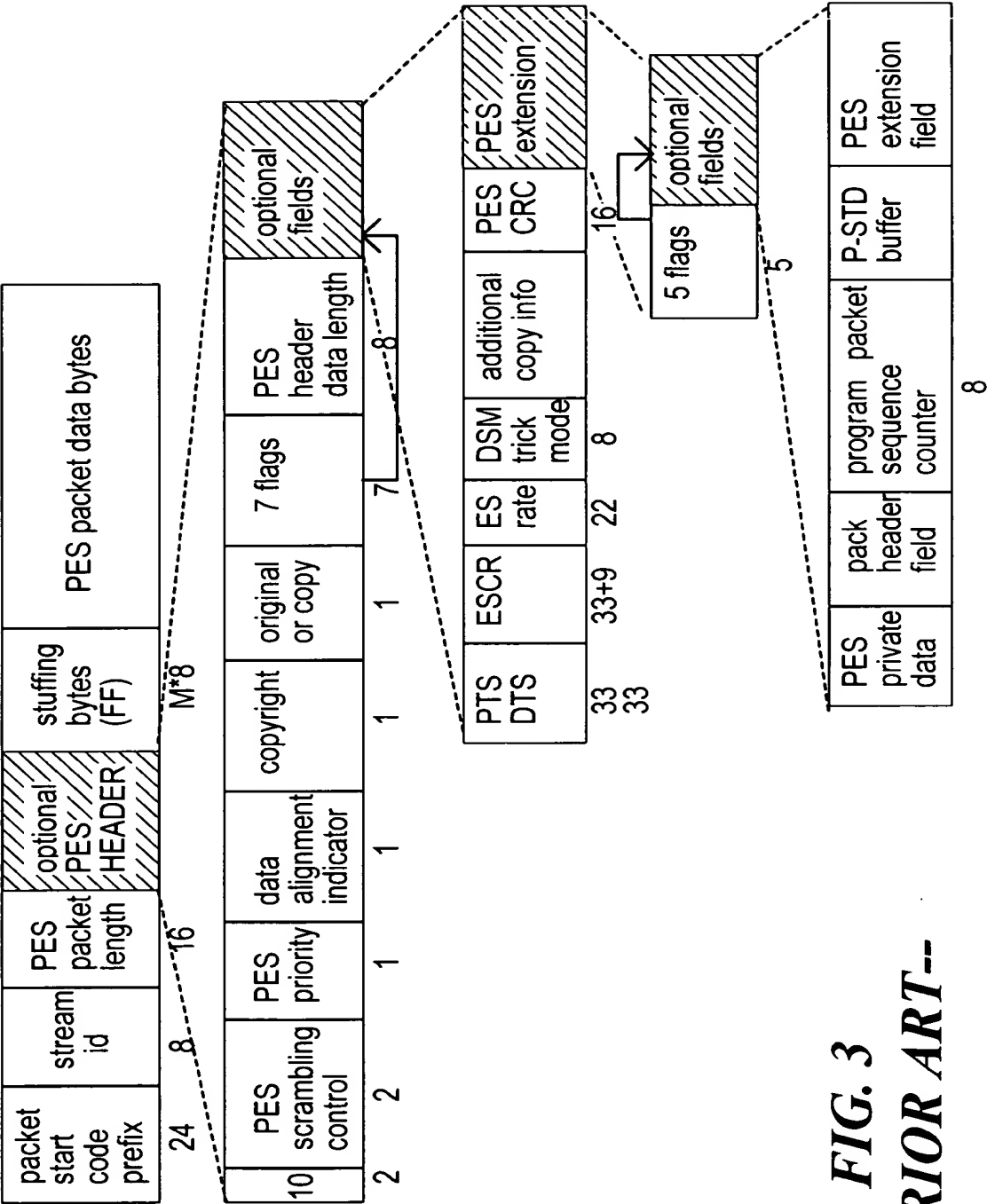


FIG. 3
---PRIOR ART---

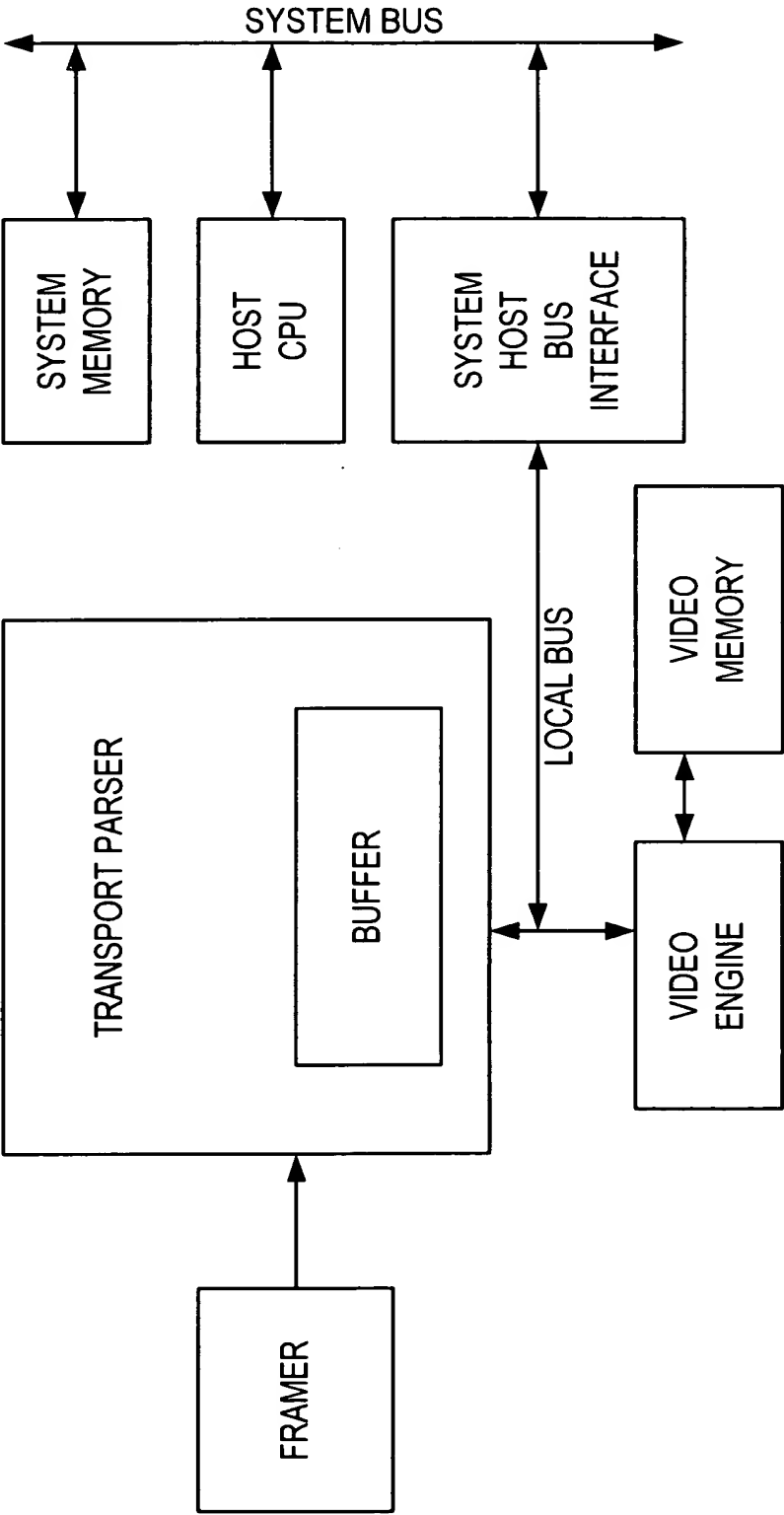


FIG. 4
--PRIOR ART--



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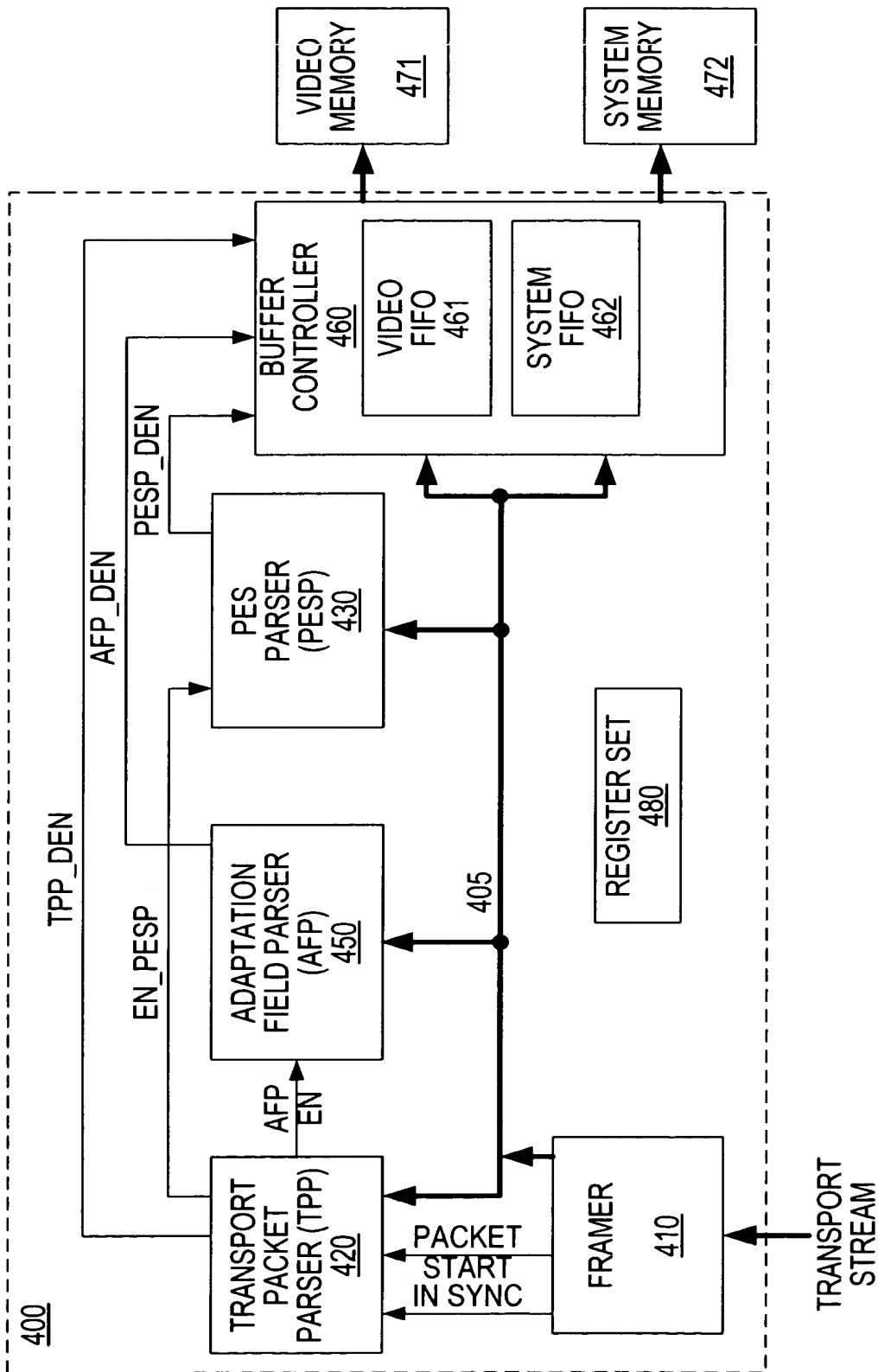


FIG. 5



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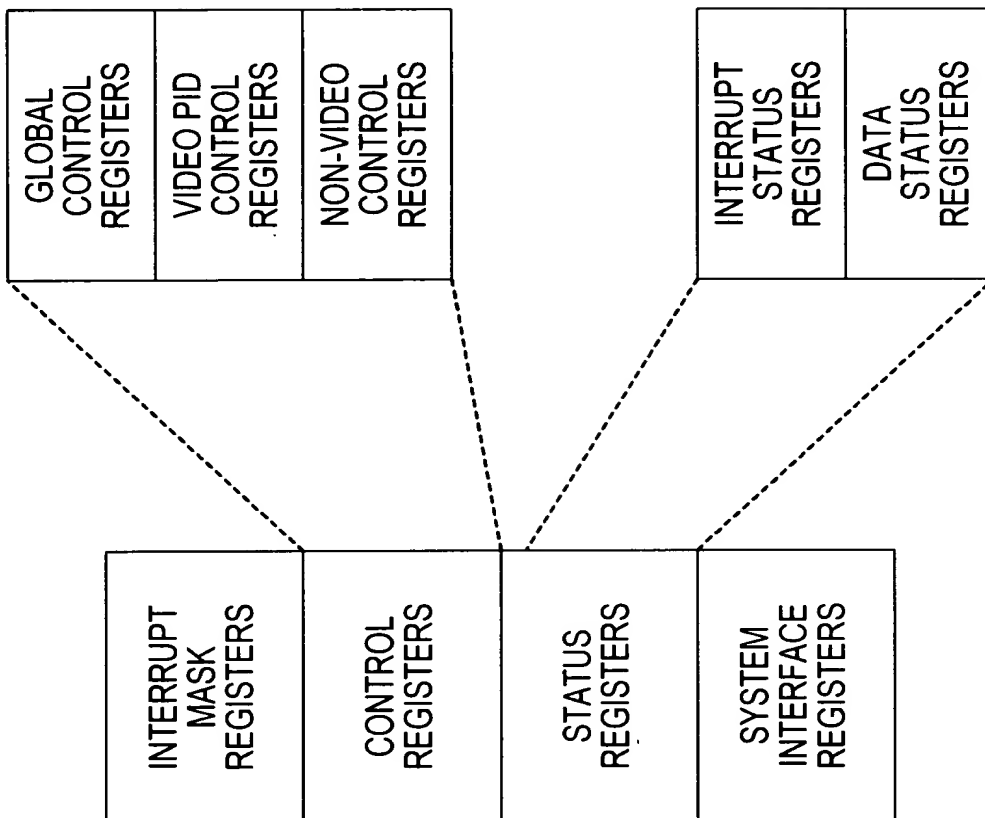


FIG. 6



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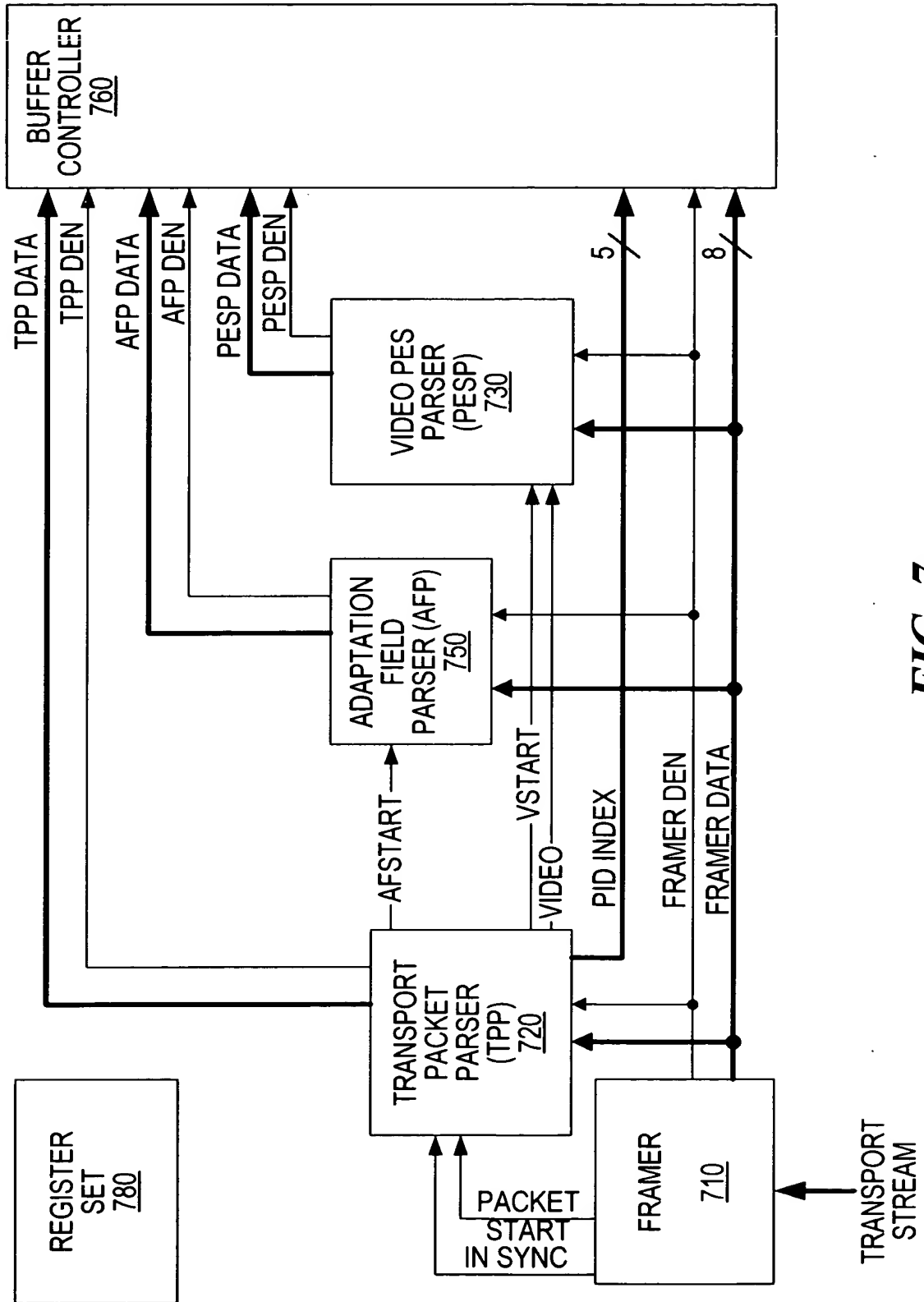


FIG. 7

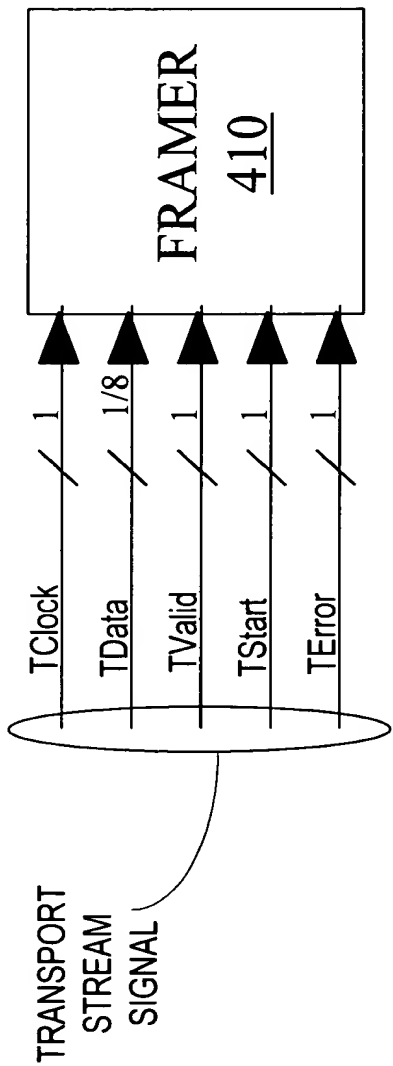


FIG. 8

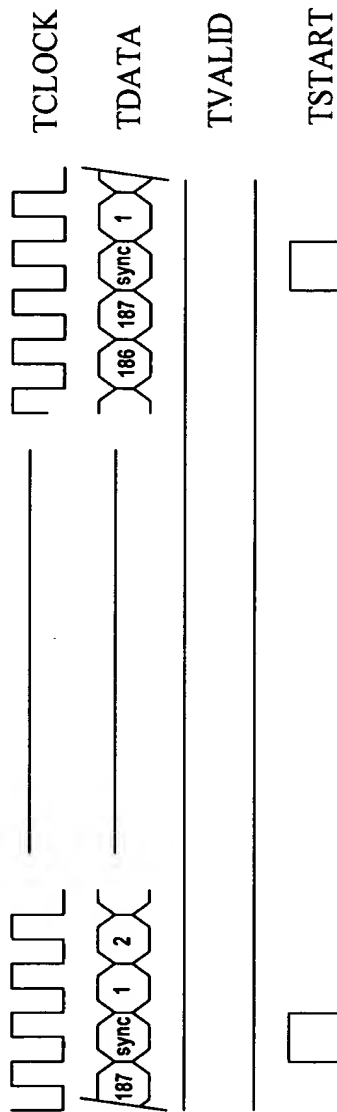
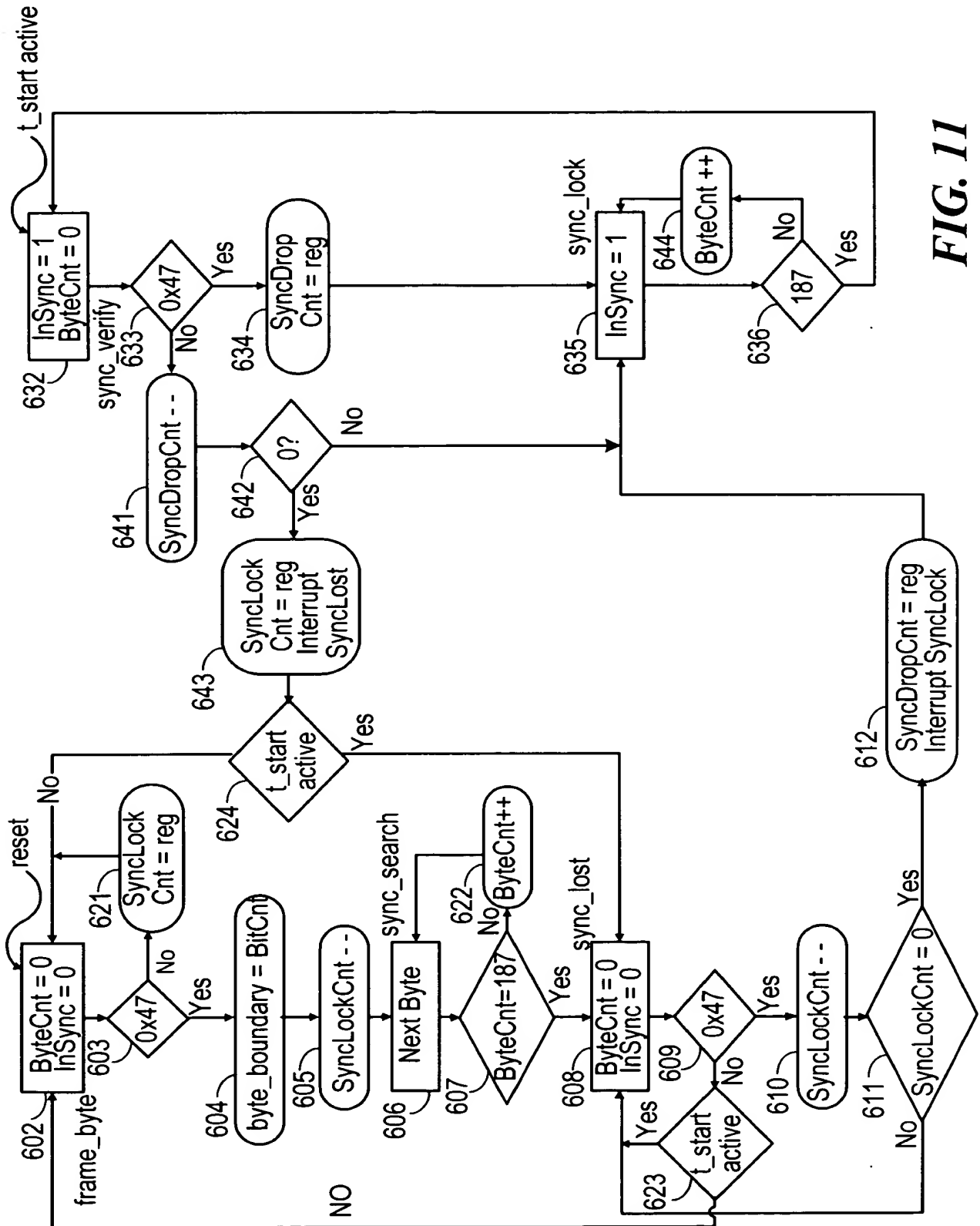


FIG. 9



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Transport Demultiplexer Global Status Register			
Field Name	Bits	Len Default	Type Description
FramerSyncLock	0	[1] 0	R/W This bit is set to '1' after the frame synchronization has been acquired. WR_ACC_CLEAR.
FramerSyncDrop	1	[1] 0	R/W This bit is set to '1' after the frame synchronization has been lost. WR_ACC_CLEAR.
CurrentFramerState	20-22 [3]	'000'	R This 3 bit field codes the current state of the framer: '000' – Capturing a byte '001' – Out of TP frame synchronization '010' – Searching for synchronization '011' – Checking for synchronization '100' – In the TP frame synchronization NOTE: Only a framer state machine updates this field. Write access does not modify it.
UnusedField	29-31 [3]	'000'	R/W Unused and reserved field.

FIG. 12



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Transport Demultiplexer Interrupt Mask Register				
Field Name	Bits	Len	Default	Type
EventInterruptMask	0-18	[19]	0	RW
				Description
				If set to '1' enables local sources of interrupts.
				Bit 0 – FramerSyncLock
				Bit 1 – FramerSyncDrop
				Bits 2 – 19 Other Functionality
EnableGlobalDemuxInterrupt	20	[1]	0	RW
UnusedField	21-31	[11]	0	RW

FIG. 13



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Transport Demultiplexer Global Control Register			
Field Name	Bits	Len Default	Type Description
FramerSyncLockLength	0-4 [5]	00101	R/W Five bits field to select a number of consecutive transport packets after MPEG-2 frame (bit-stream) synchronization is declared.
FramerSyncDropLength	5-7 [3]	011	R/W Three bits field to select a number of consecutive transport packets after a loss of MPEG-2 frame synchronization is declared.
FramerBitPolarity	8 [1]	0	R/W '0' selects msb first (default mode), '1' select lsb first
FramerClockPolarity	9 [1]	0	R/W If set to '0' framer will latch on falling edge (default) If set to '1' framer will latch on rising edge.
FramerMode:	10-11 [2]	'00'	R/W Defines a combination of external control signals: '00' – Framer uses T_start only. '01' – Framer uses T_valid only. '10' – Framer uses T_start and T_valid. '11' – Framer uses T_clock and T_data only.
Other Functionality Bits	12-15 [4]		Other functionality (not relevant to Framer)
T_ValidPolarity	16 [1]	1	R/W '1' selects active high [5V] for t_valid external signal
T_StartPolarity	17 [1]	1	R/W '1' selects active high [5V] for t_start external signal
T_ErrorPolarity	18 [1]	1	R/W '1' selects active high [5V] for t_error external signal
Other Functionality Bits	19-28 [10]		Other functionality (not relevant to Framer)
UnusedField	29-31 [3]	0	R/W Unused and reserved field. Always set to 0.

FIG. 14



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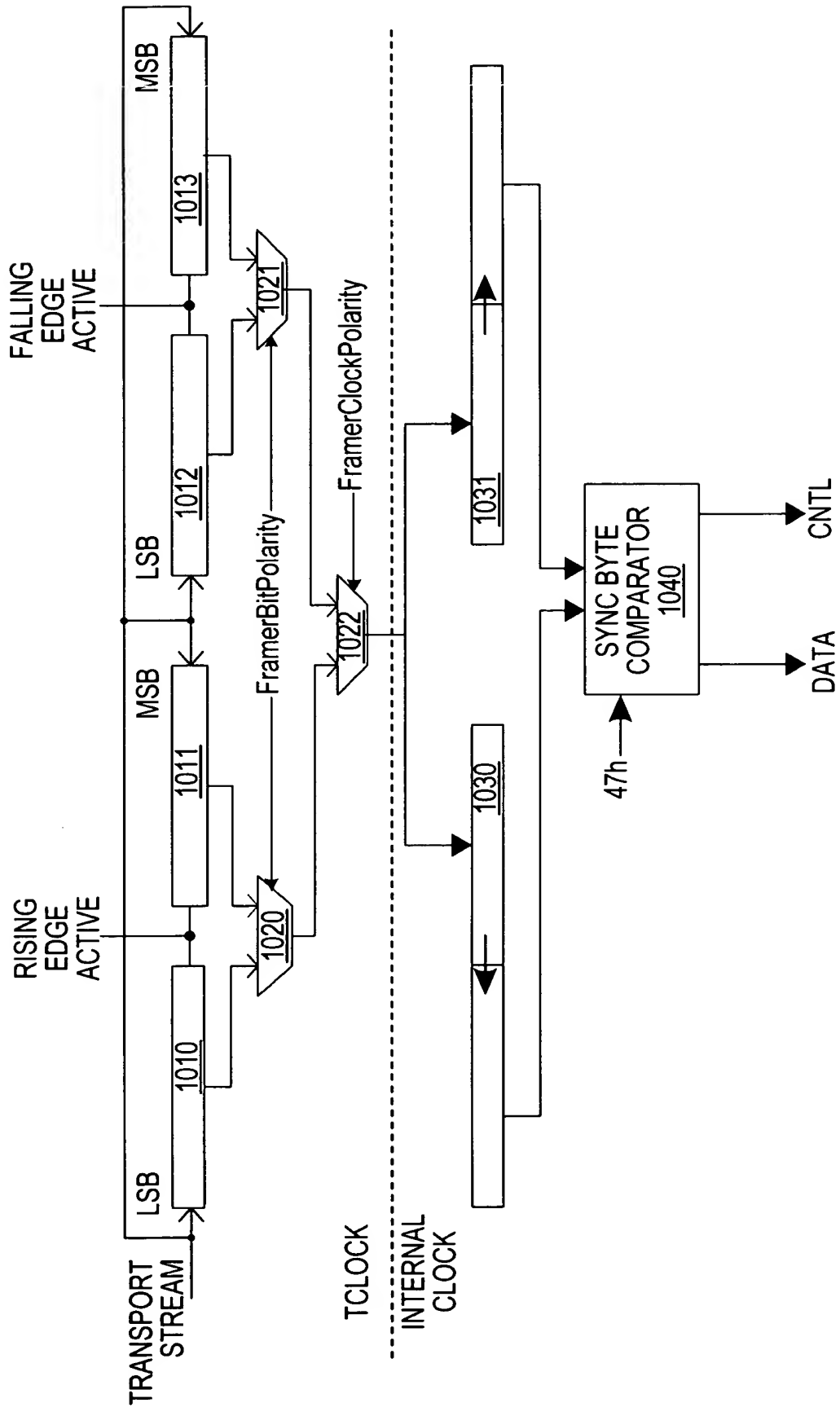


FIG. 15

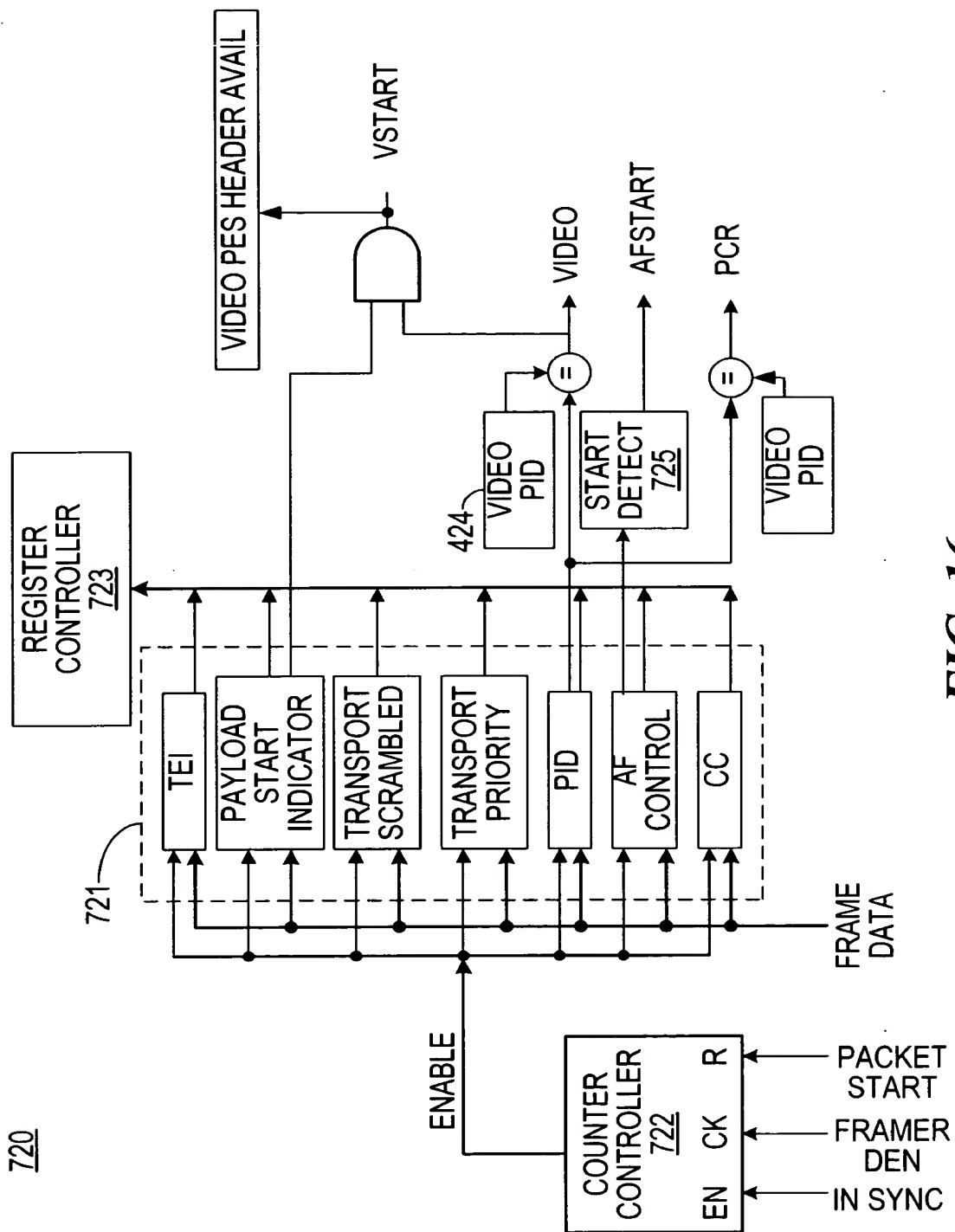
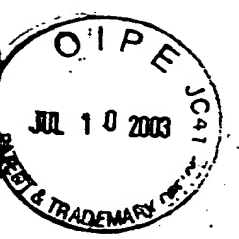


FIG. 16



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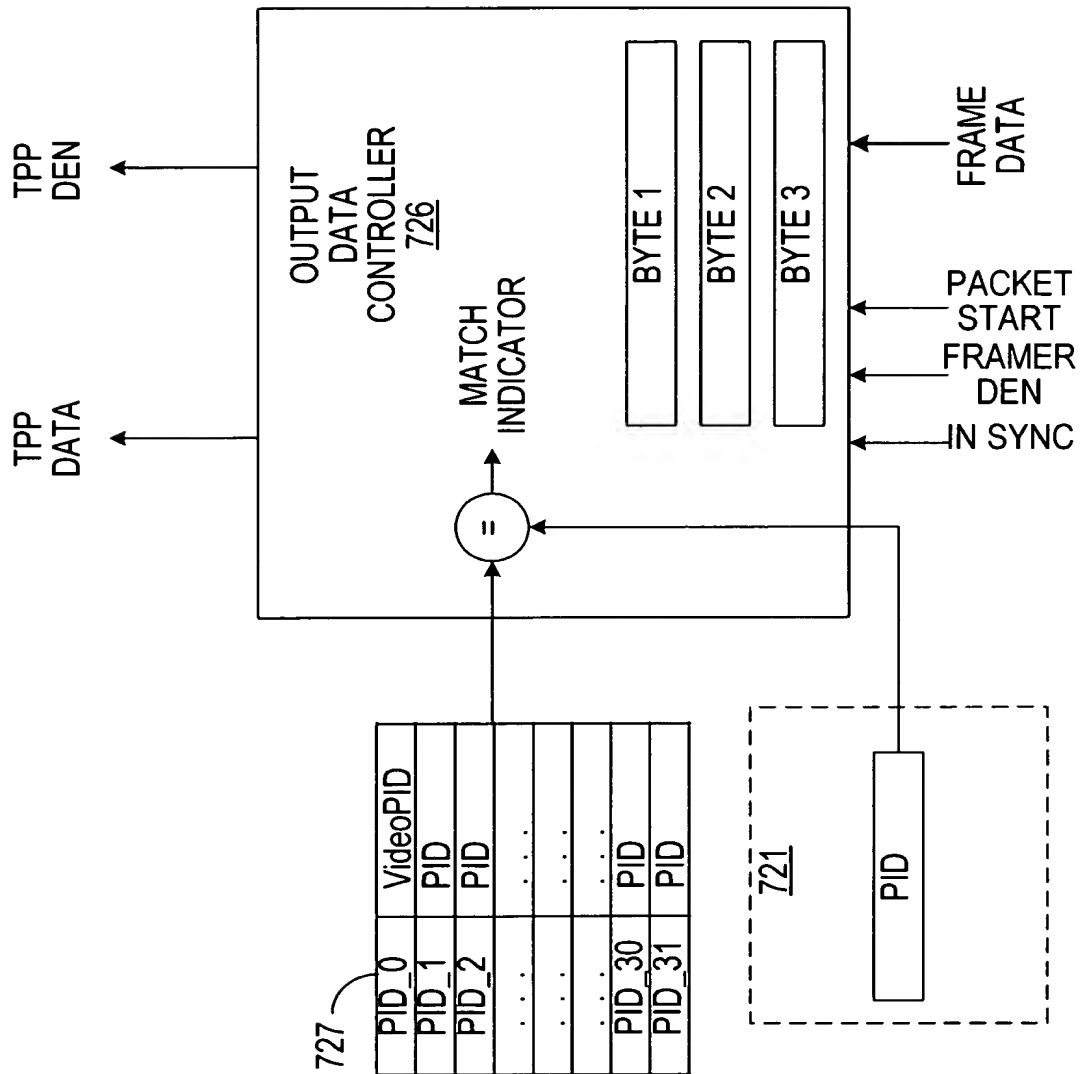


FIG. 17



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Video Control Registers					
Field Name	Bits	Len	Default	Type	Description
VideoPid	0-12	[13]	0x1FFF	R/W	Selects a specific PID of the video component stream to filter on. Value of 4095 is reserved one (it means a NULL transport packets).
EnableParsing	13	[1]	0	R/W	If '1' enables parsing from the next transport packet.
StartFromPUSCommand	14	[1]	0	R/W	'0' enables PES parsing immediately. '1' enables PES parsing a transport packet from new PES packet. After that, this bit auto-returns to 0.
ProcessStreamID	15	[1]	0	R/W	If '1' enables parsing on specific stream_id field.
StreamID	16-23	[8]	0xE0	R/W	stream_id of the ES stream to filter on in the PESP.

FIG. 18

Transport Demultiplexer Registers							
Field Name		Bits	Len	Default	Type	Description	
PID_yz,		0 ≤ yz ≤ 30	0-12	[13]	0x1FFF	R/W	Selects a specific PID of the component stream to filter on. Value of 0x1FFF is reserved (it means a NULL transport packets).
EnableParsing			13	[1]	0	R/W	If set to '1' extraction of defined PID yz is enabled.
BufferIndex			14-17	[4]	0	R/W	Specifies 1 of 16 destination buffers in the sys. mem.

FIG. 19



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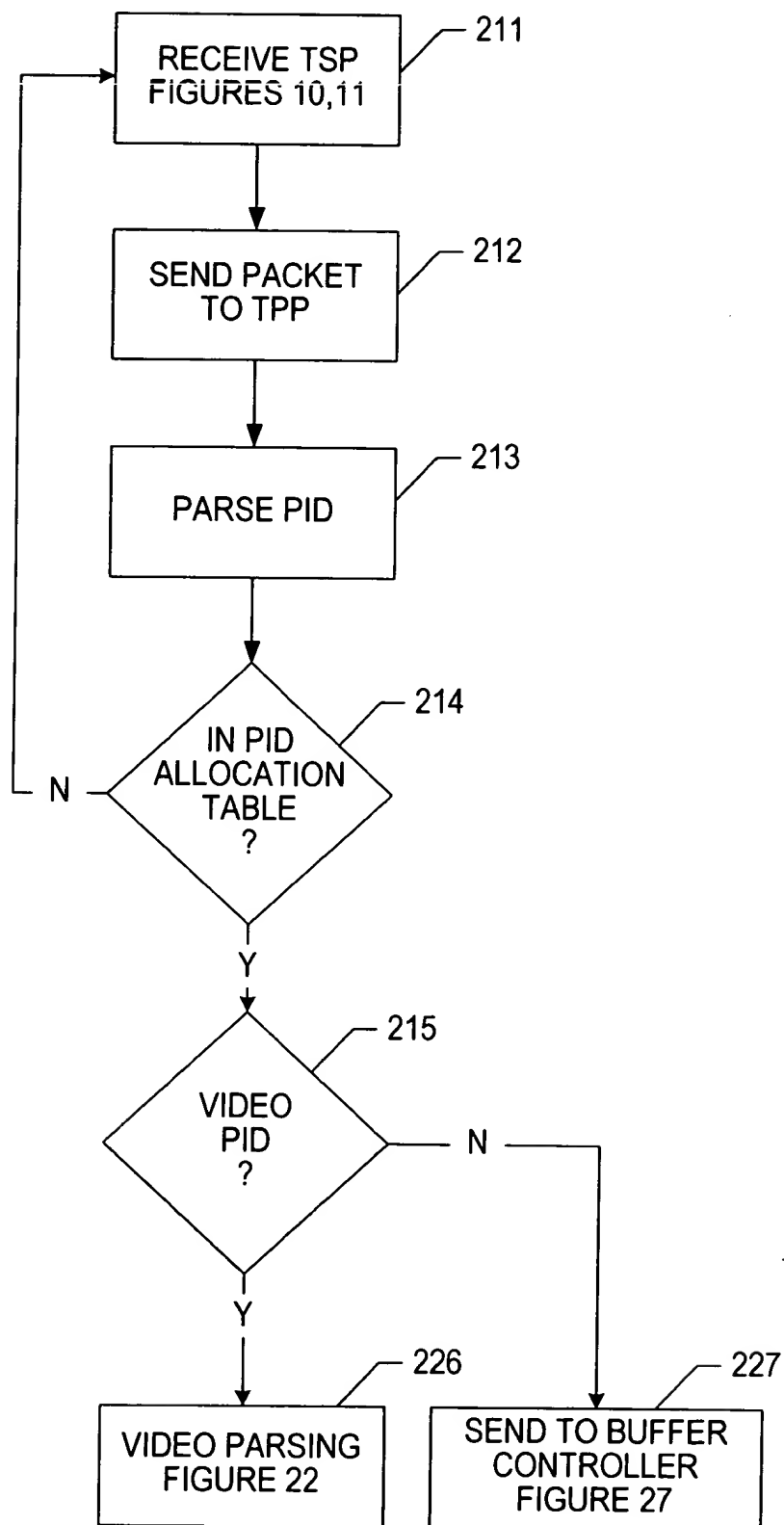


FIG. 20



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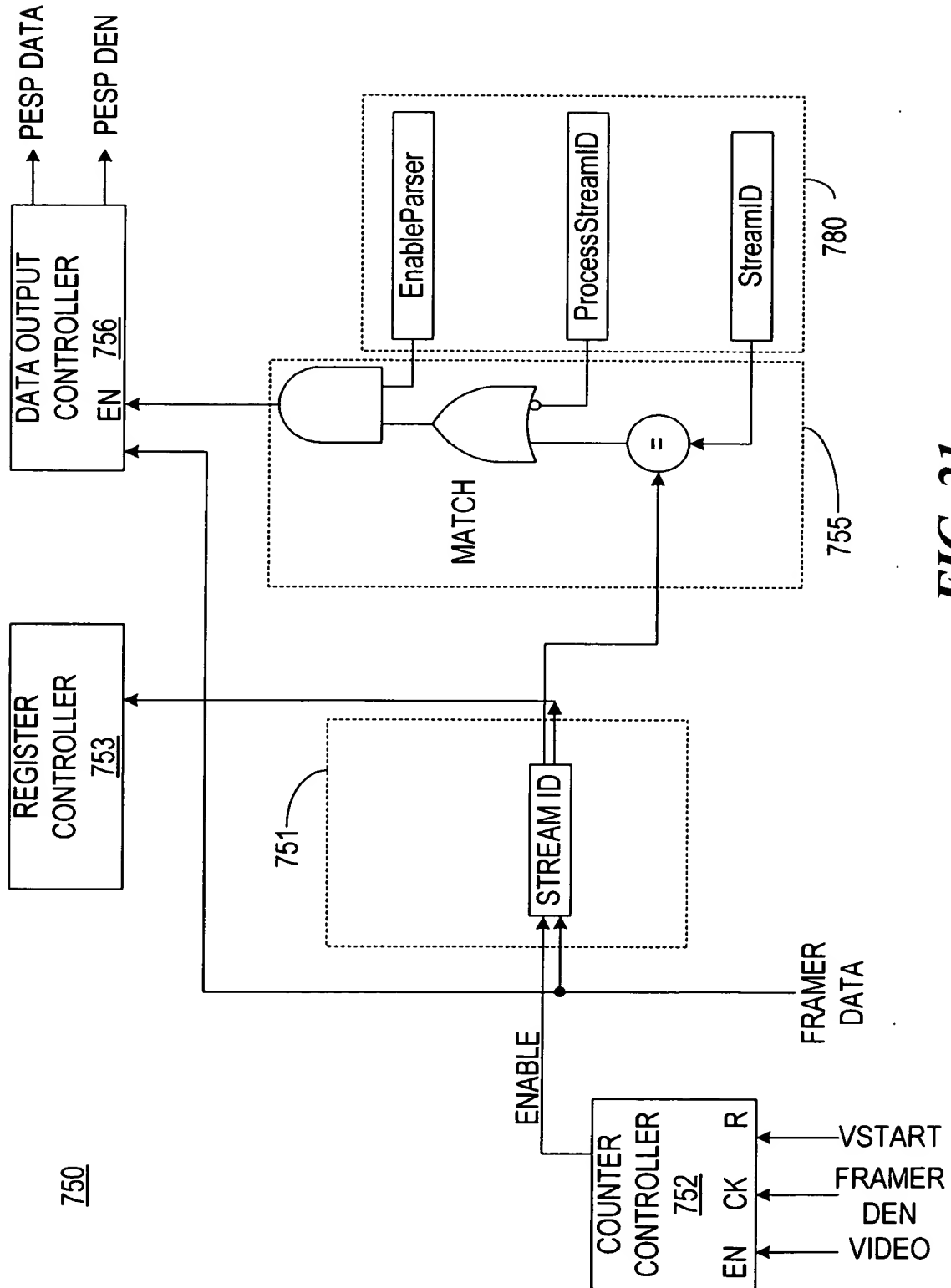


FIG. 21



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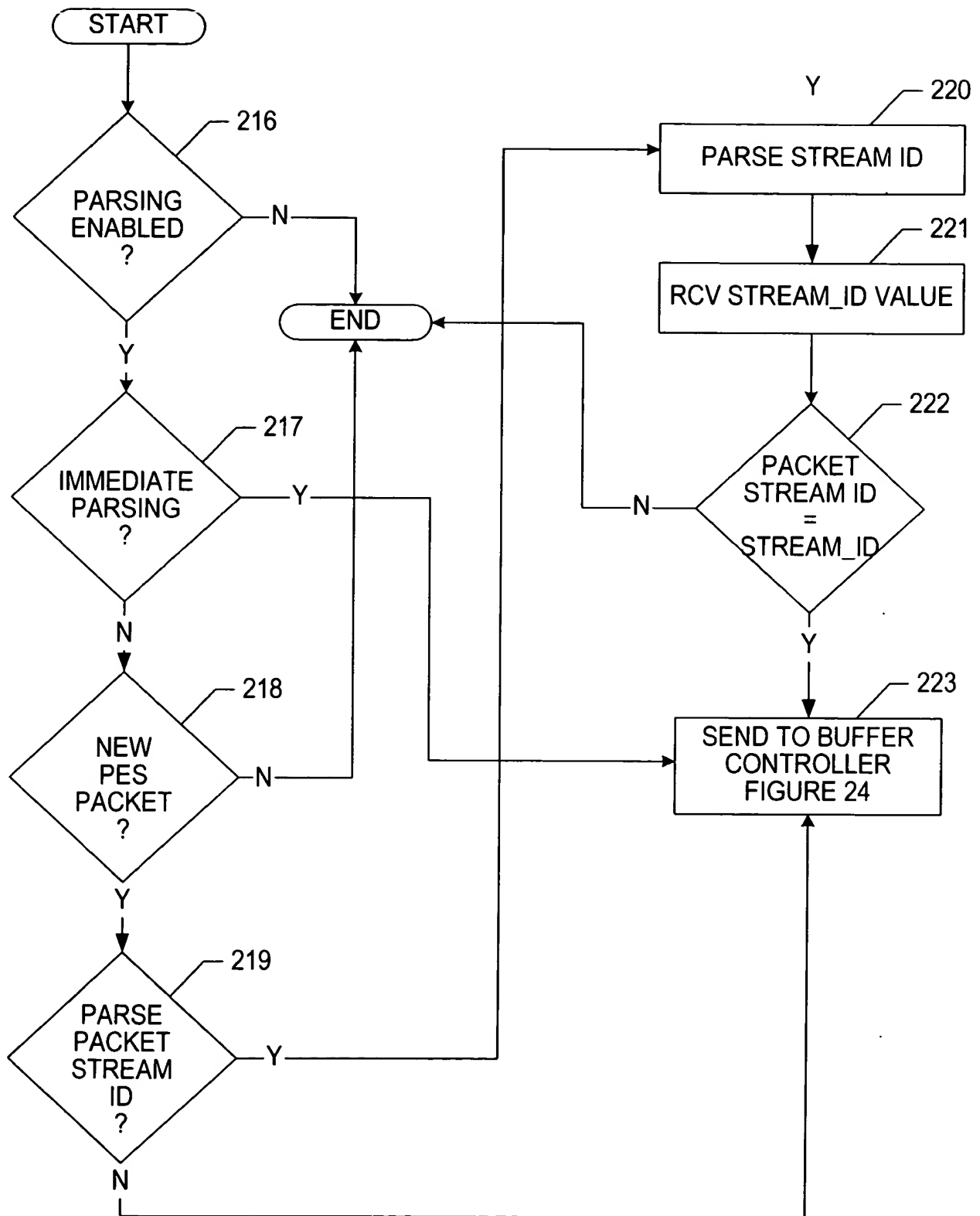
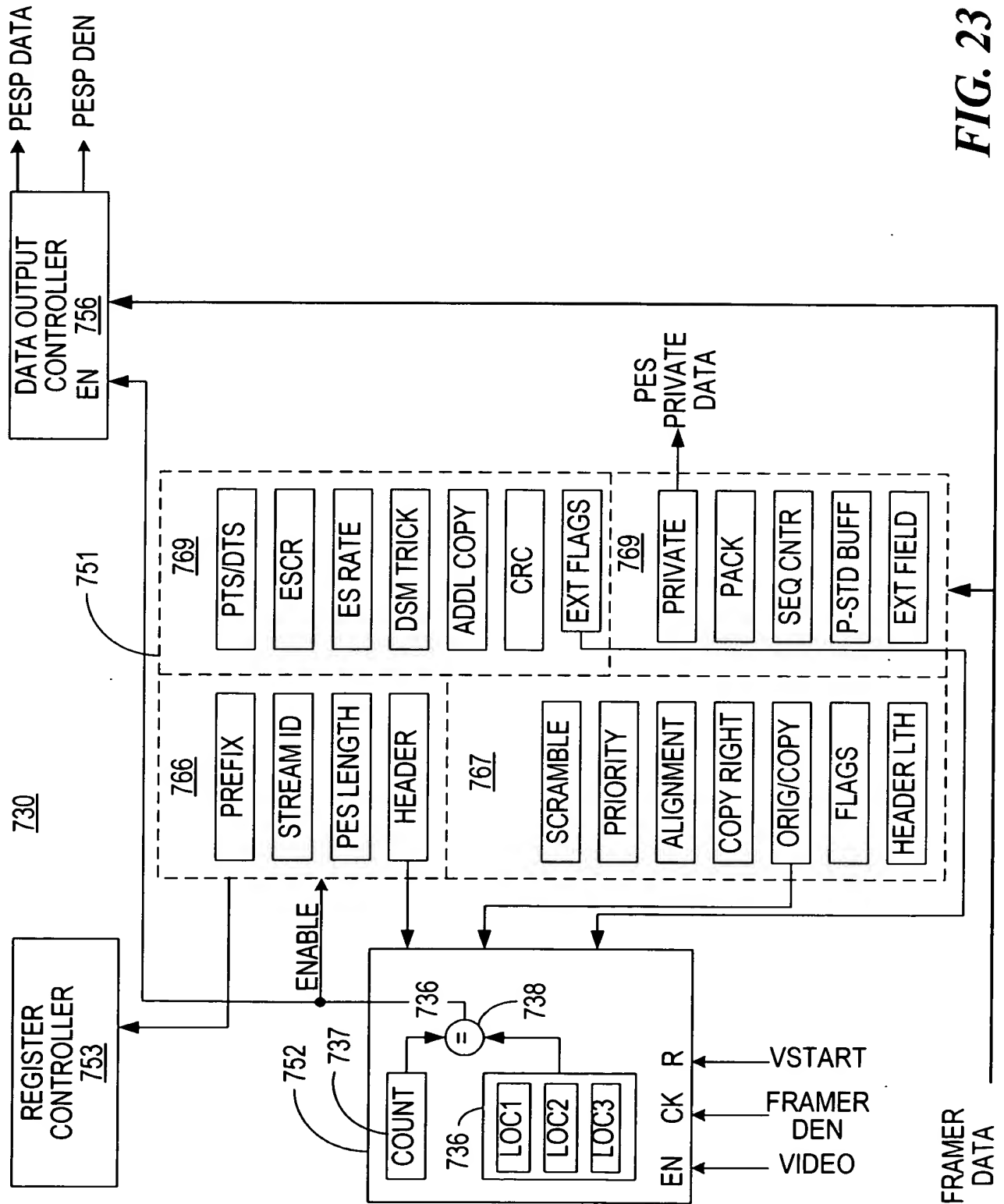


FIG. 22



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FIG. 24

Transport Demultiplexer Global Status Register			
Field Name	Bits	Len	Type
VideoPESHeaderAvailable	12	[1]	0 R/W
This bit is set to '1' when the new PES header of the video stream is received. WR ACC CLEAR.			
VideoPESHeaderError	13	[1]	0 R/W
This bit is set to '1' after an error in the PES header is found. WR ACC CLEAR.			
VideoPESDataAlignment	14	[1]	0 R/W
This bit is set to '1' when video PID has AF data_alignment_flag, indicating a possible start of I frame. WR ACC CLEAR.			
VideoPESDSMTTrickMode	15	[1]	0 R/W
Indicates that DSM data is found and extracted. WR ACC CLEAR.			
VideoPESPrivateData	16	[1]	0 R/W
This bit is set to '1' when video PID has 16 bytes of private data in the PES header. WR ACC CLEAR.			
VideoPESCRCErr	17	[1]	0 R/W
This bit is set to '1' if the video CRC of the PES parser found a CRC mismatch. WR ACC CLEAR.			

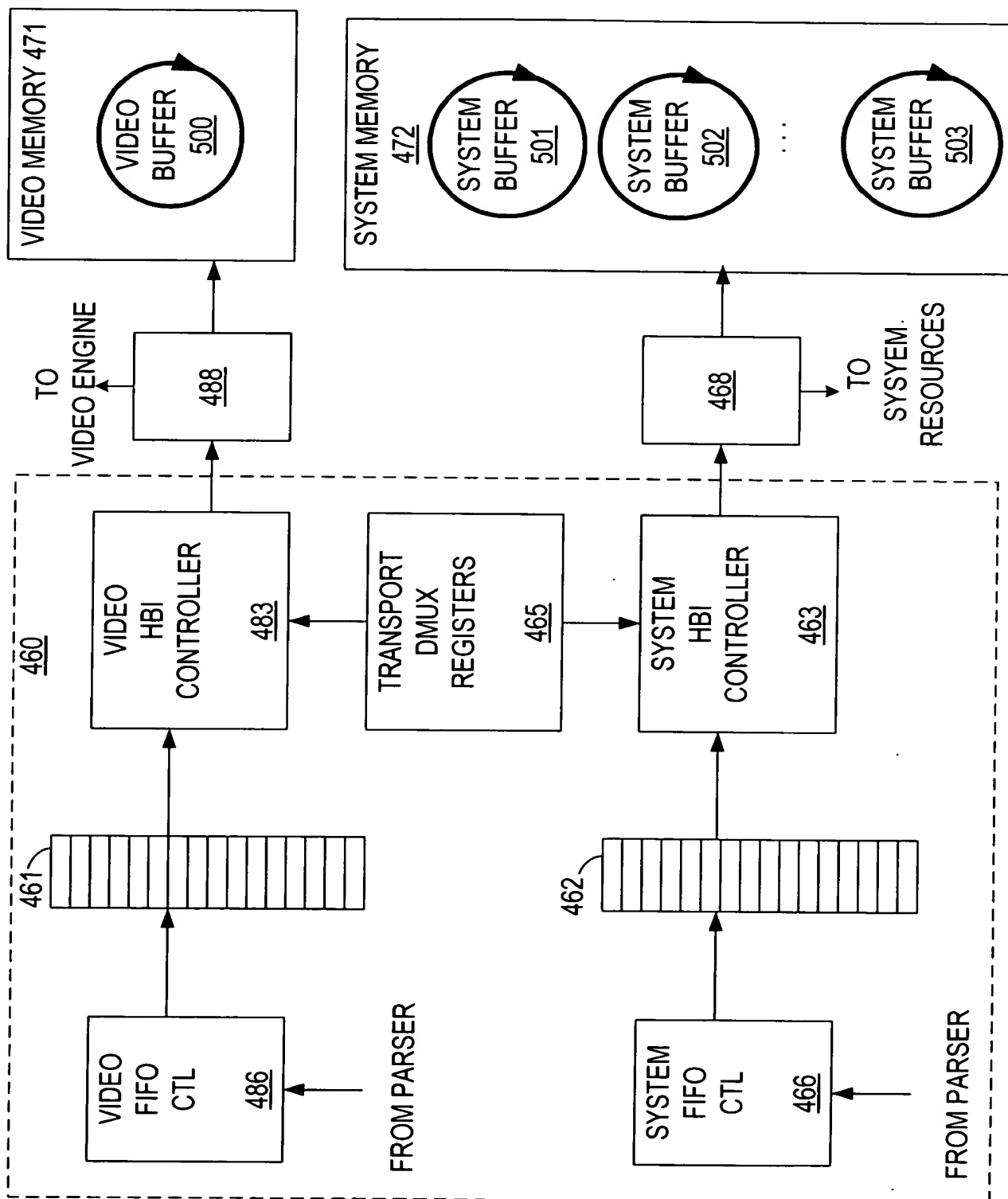
FIG. 25

Transport Demultiplexer Interrupt Mask Register			
Field Name	Bits	Len	Type
EventInterruptMask	0-18	[19]	0 R/W
If set to '1' enables local sources Bit 12 – VideoPESHeaderAvailable Bit 13 – VideoPESHeaderError Bit 14 – VideoPESDataAlignment Bit 15 – VideoPESDSMTTrickMode Bit 16 – VideoPESPrivateData Bit 17 – VideoPESCRCErr Bit 18 – VideoPTSRReceived Bit 19 – VideoESCRRReceived			



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FIG. 26





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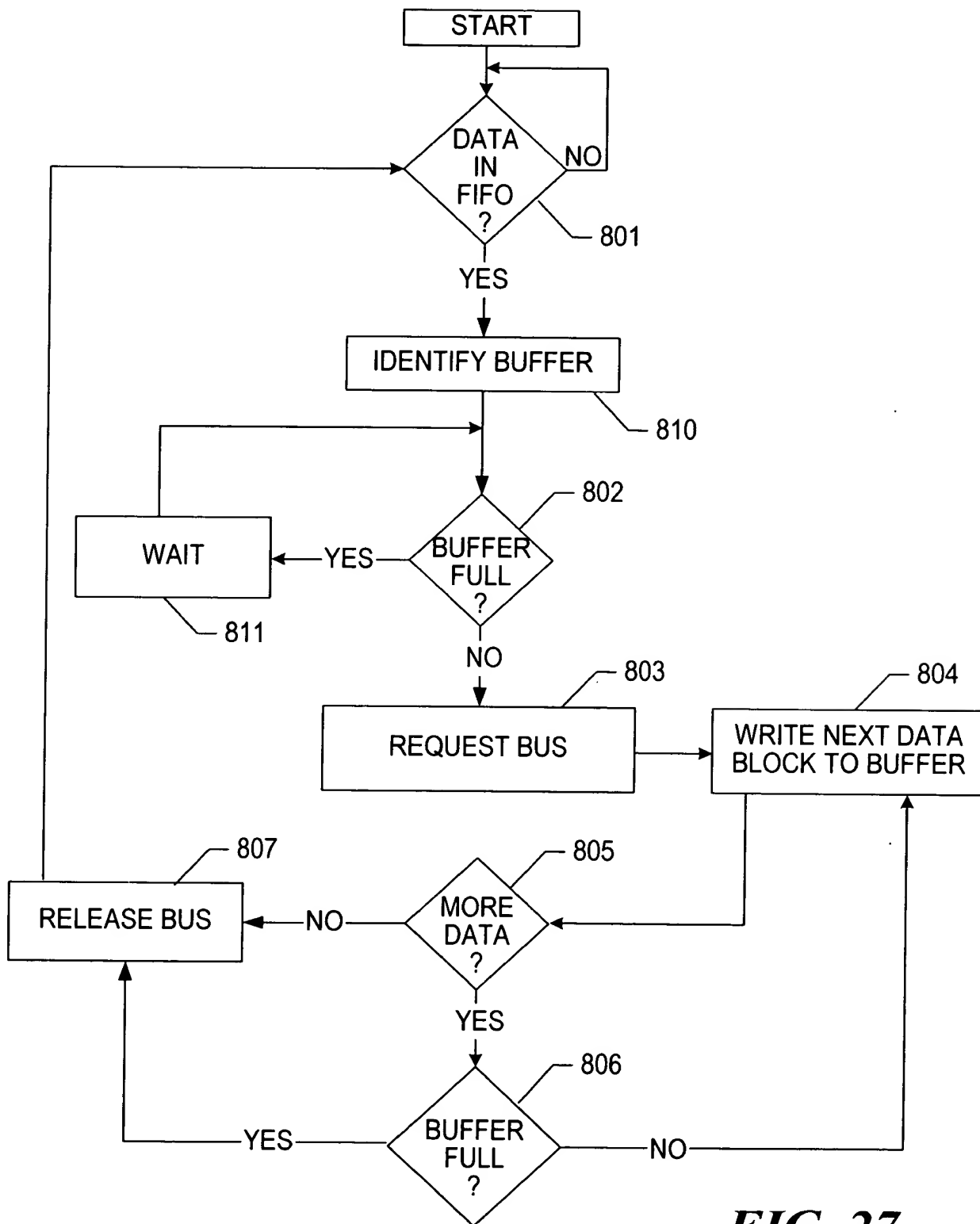
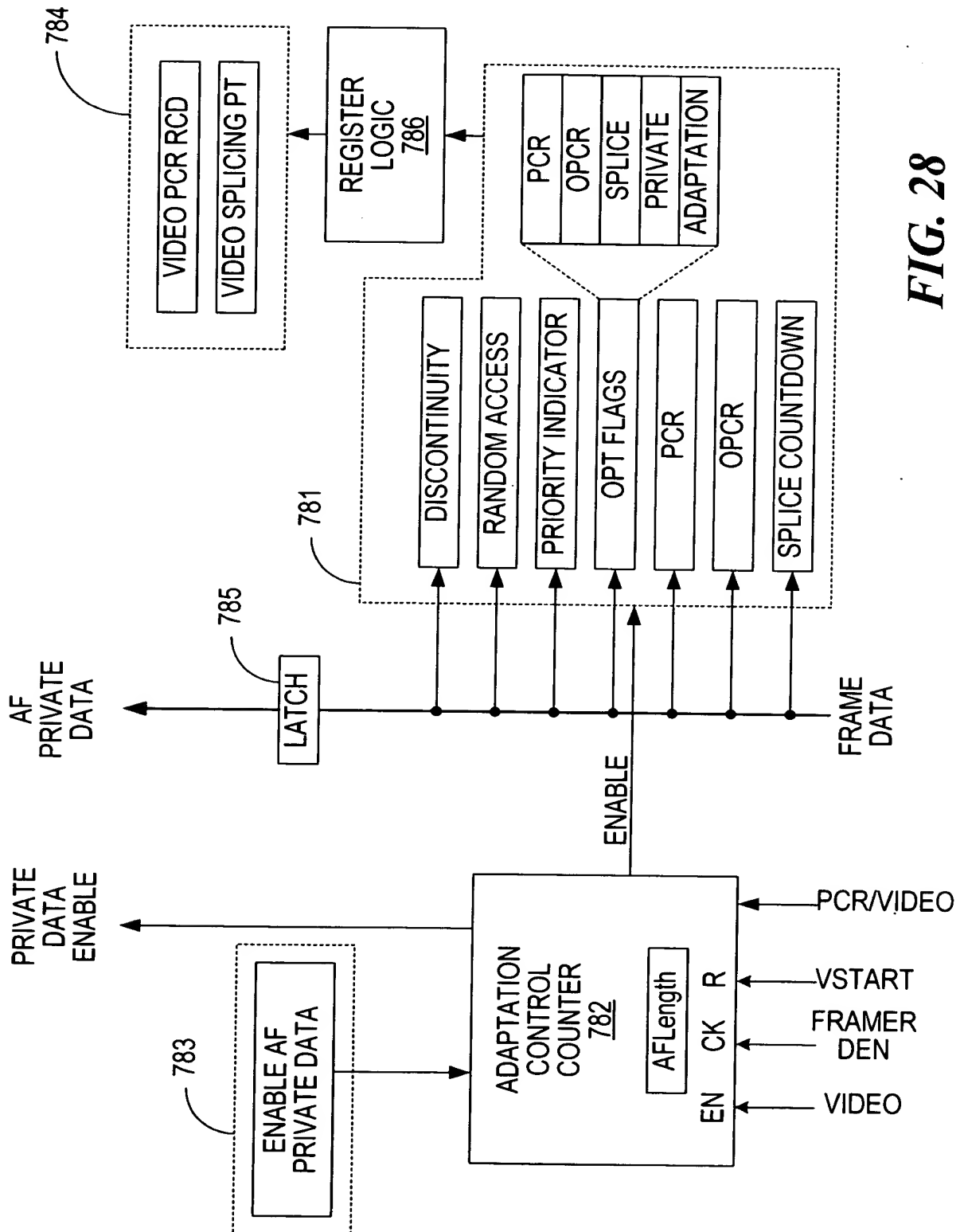


FIG. 27



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Transport Demultiplexer Global Status Register				Description
Field Name	Bits	Len	Default	
VideoAFPcrReceived	[1]	0		This bit is set to '1' after arrival and extraction of PCR sample in the adaptation field. WR ACC CLEAR.
VideoAFPcrDiscontinuity	[1]	0		This bit is set to '1' when a <i>discontinuity_indicator</i> in The adaptation field of the PCR PID is asserted. WR ACC CLEAR.
VideoAFDiscontinuityFlag	[1]	0		This bit is set to '1' after a <i>discontinuity_indicator_flag</i> has been asserted in the AF of video TP, indicating a discontinuity on continuity_counter. WR ACC CLEAR.
VideoAFRandomAccess	[1]	0		This bit is set to '1' when video PID has <i>random_access_flag</i> asserted in the AF, indicating a start of the elementary stream. WR ACC CLEAR.
VideoAFSplicingFlag	[1]	0		This bit is set to '1' when video PID has <i>splicing_point_flag</i> asserted in the AF, indicating approaching of the splicing point. WR ACC CLEAR.
VideoAFSplicingPoint	[1]	0		This bit is set to '1' when video PID has <i>splicing_point_flag</i> asserted in the AF, after splicing point occurred (<i>splice_countdown</i> = 0). WR ACC CLEAR.
VideoAFPrivateData	[1]	0		This bit is set to '1' when video has AF private data. WR ACC CLEAR.
AFSpliceCountdown	[8]	0x00		Current splice countdown value from adaptation field of AV packets. Modified on the fly by AF content

FIG. 29



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Transport Demultiplexer Interrupt Mask Register			
Field Name	Bits	Len	Type
EventInterruptMask	0-18	[19]	0 R/W
			Description If set to '1' enables local sources Bit 5 – VideoAFPCrReceived Bit 6 – VideoAFPCrDiscontinuity Bit 7 – VideoAFDiscontinuityFlag Bit 8 – VideoAFRandomAccessFlag Bit 9 – VideoAFSplicingFlag Bit 10 – VideoAFSplicingPoint Bit 11 – VideoAFPrivateData

FIG. 30

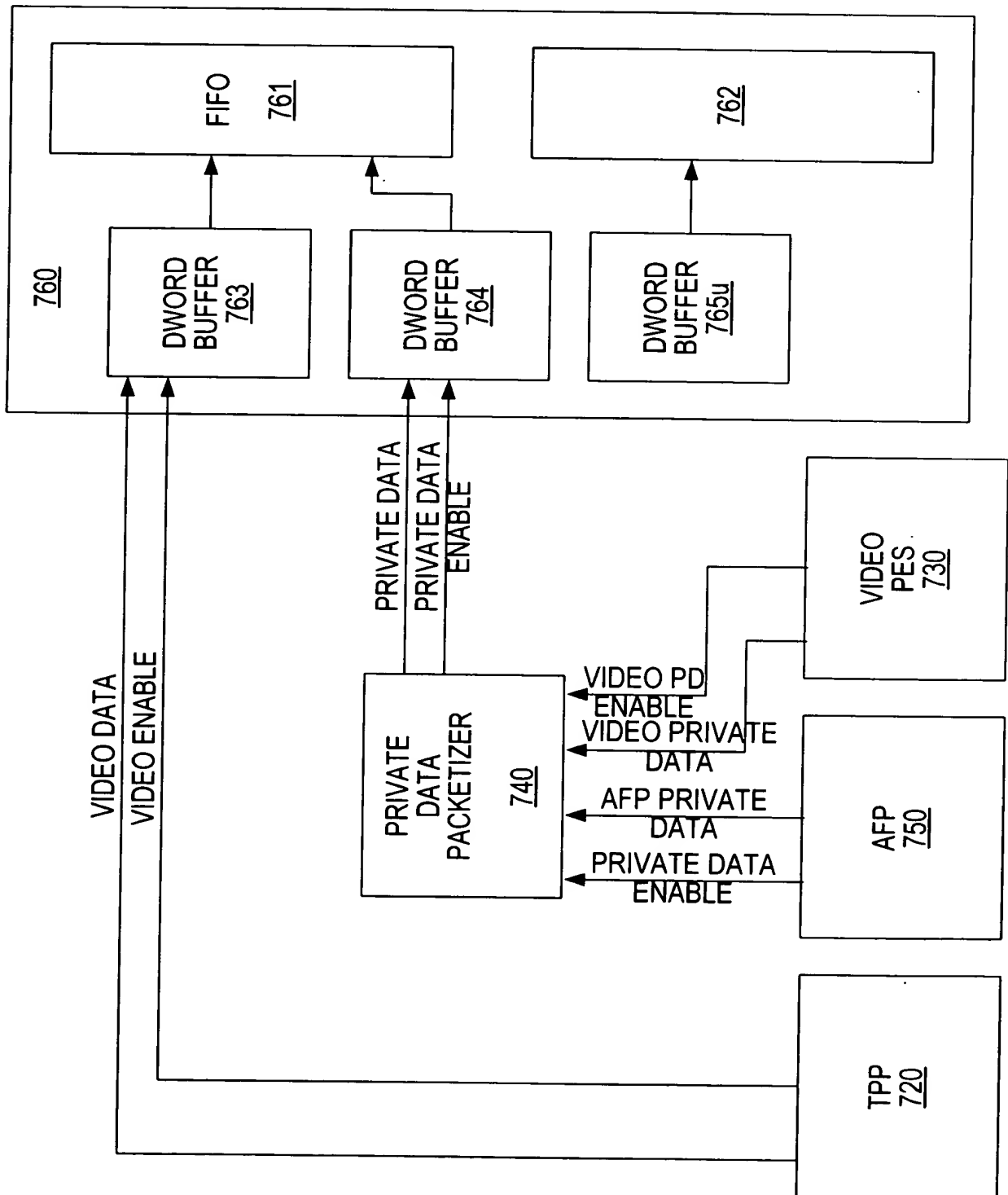
Transport Demultiplexer Global Control Register			
Field Name	Bits	Len	Type
EnableAFPrivateData	[1]	0	R/W
AFPrivateDataBufferIndex	[4]	0	R/W
PCRIndex	[1]	0	R/W
EnableAutoSplicing	[1]	0	R/W
			Description If '1' enables parsing and routing of AF private data Specifies 1 of 15 destination buffers in the system memory

FIG. 31



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FIG. 32



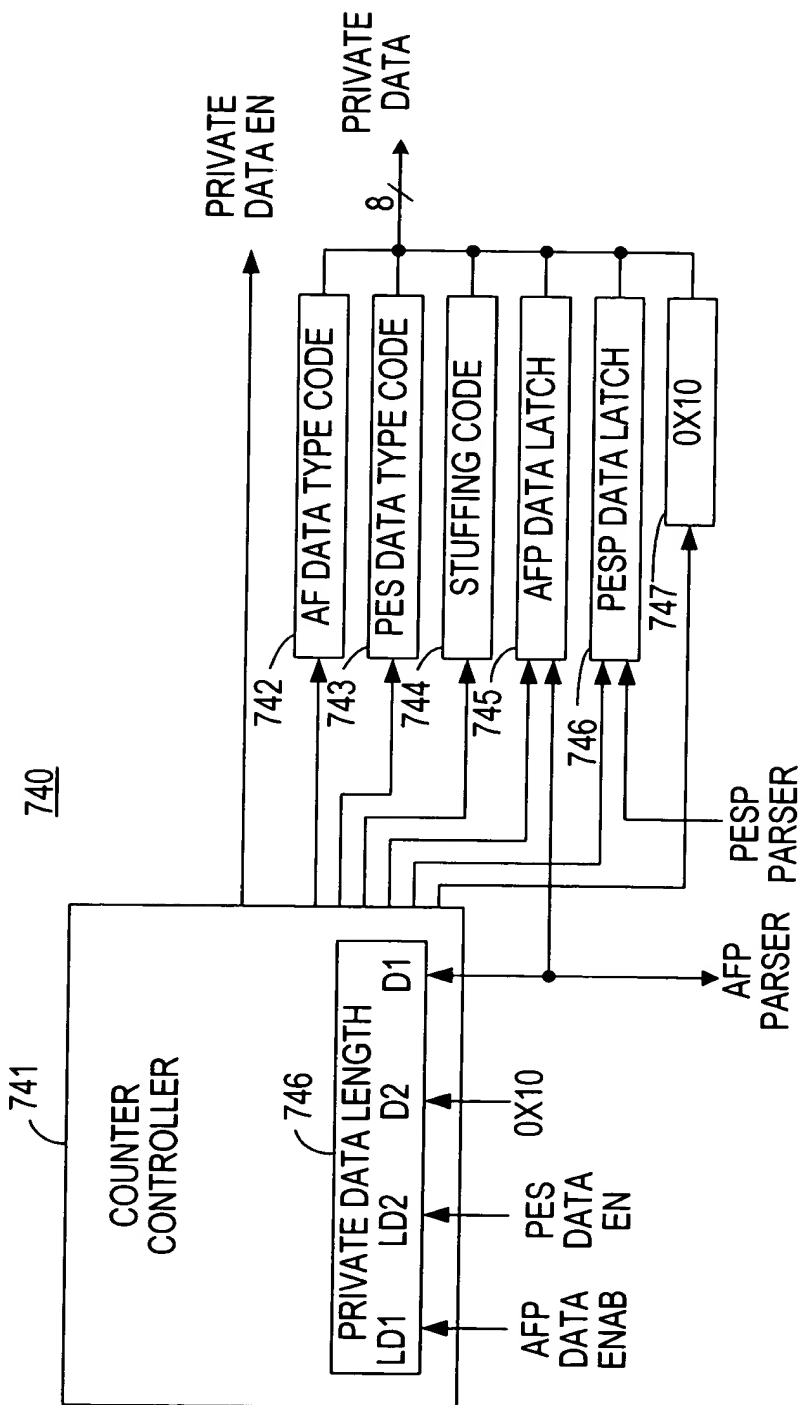


FIG. 33

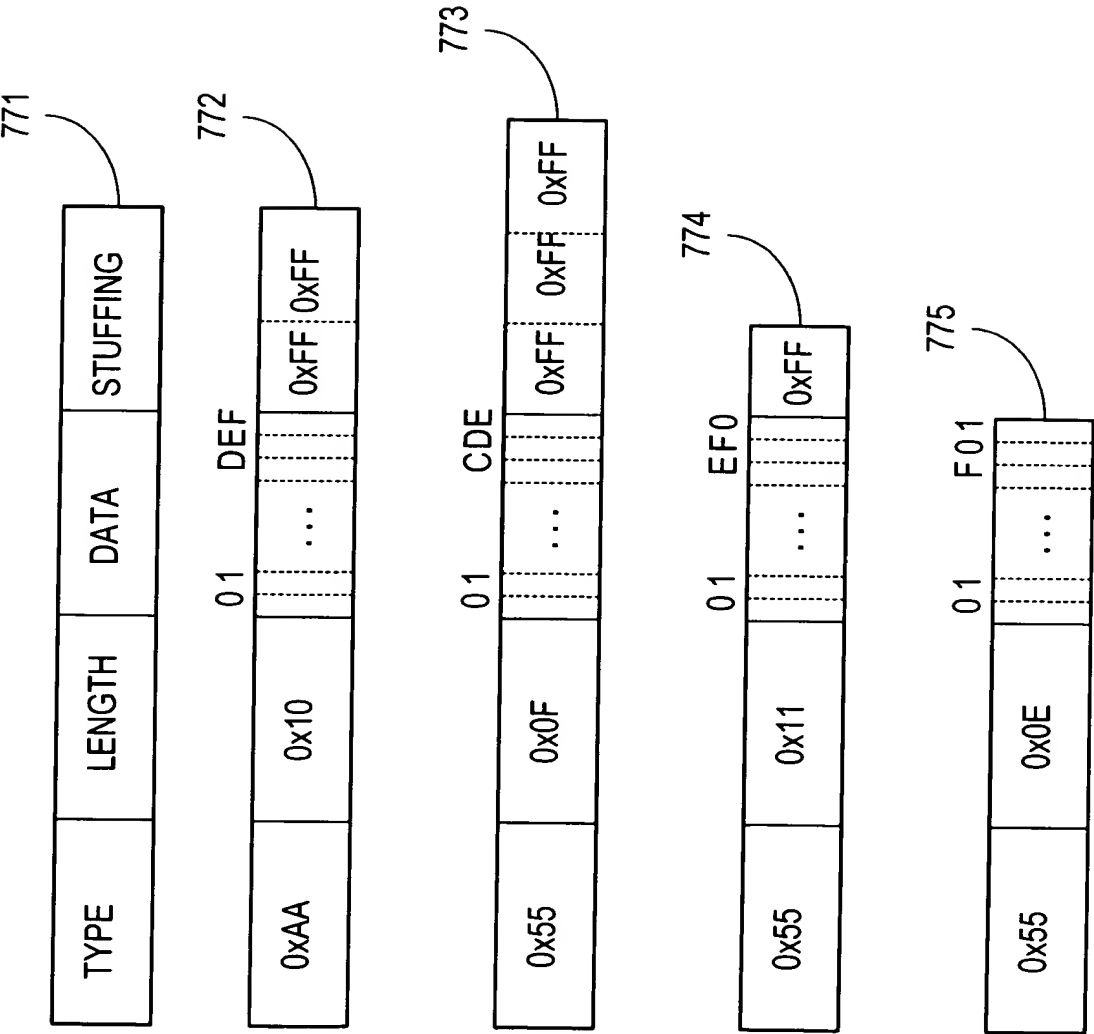


FIG. 34



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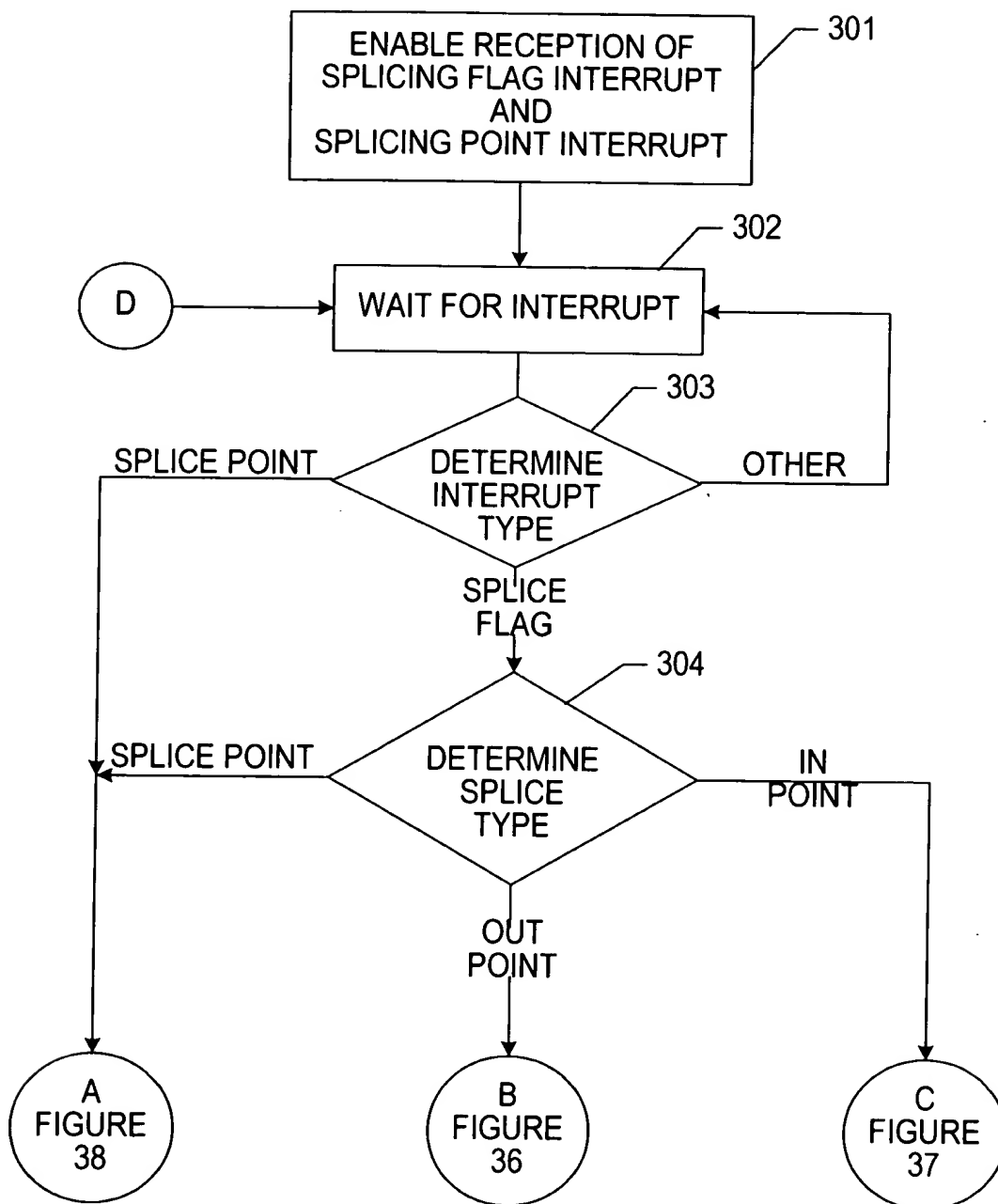


FIG. 35



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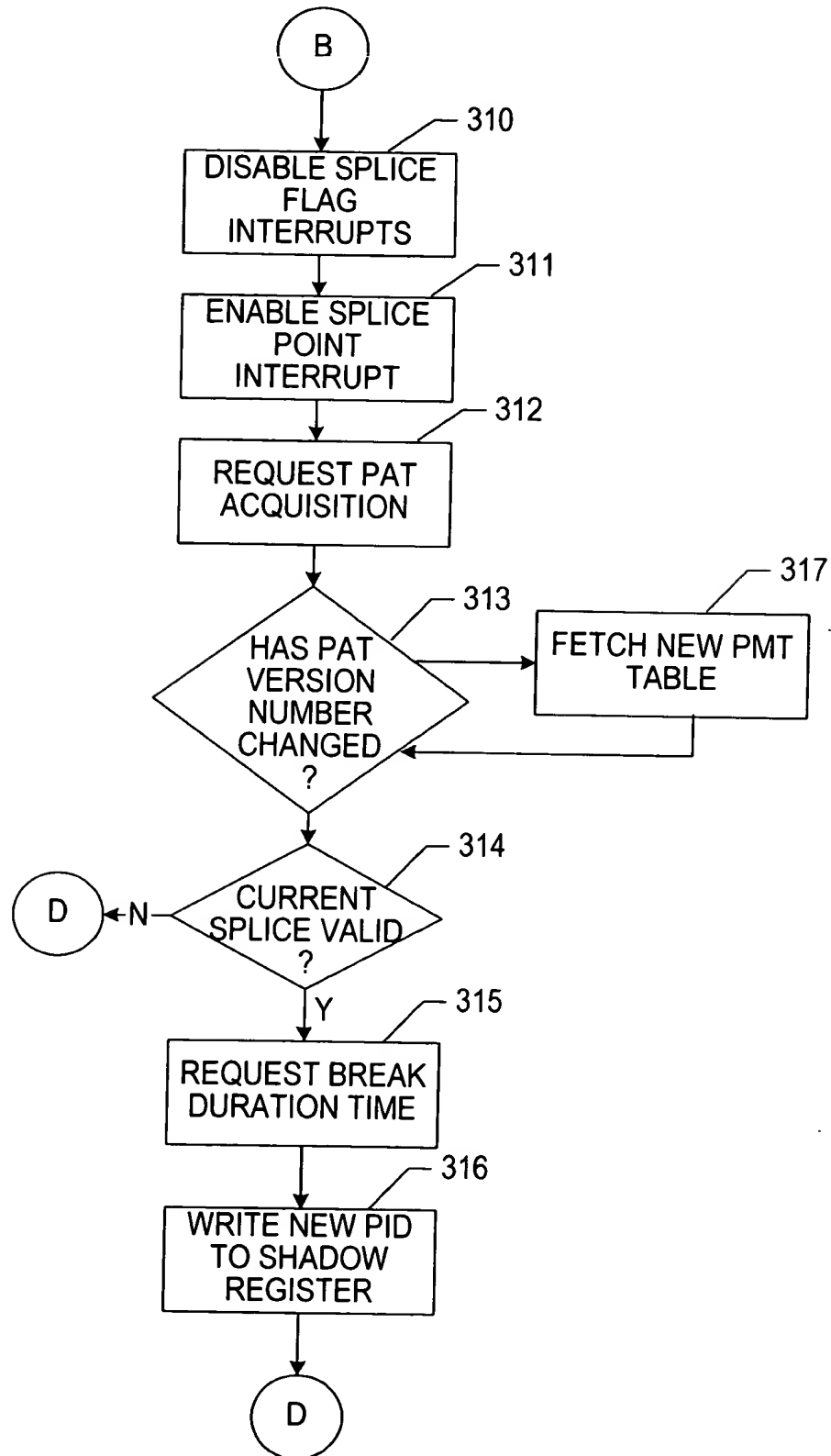


FIG. 36



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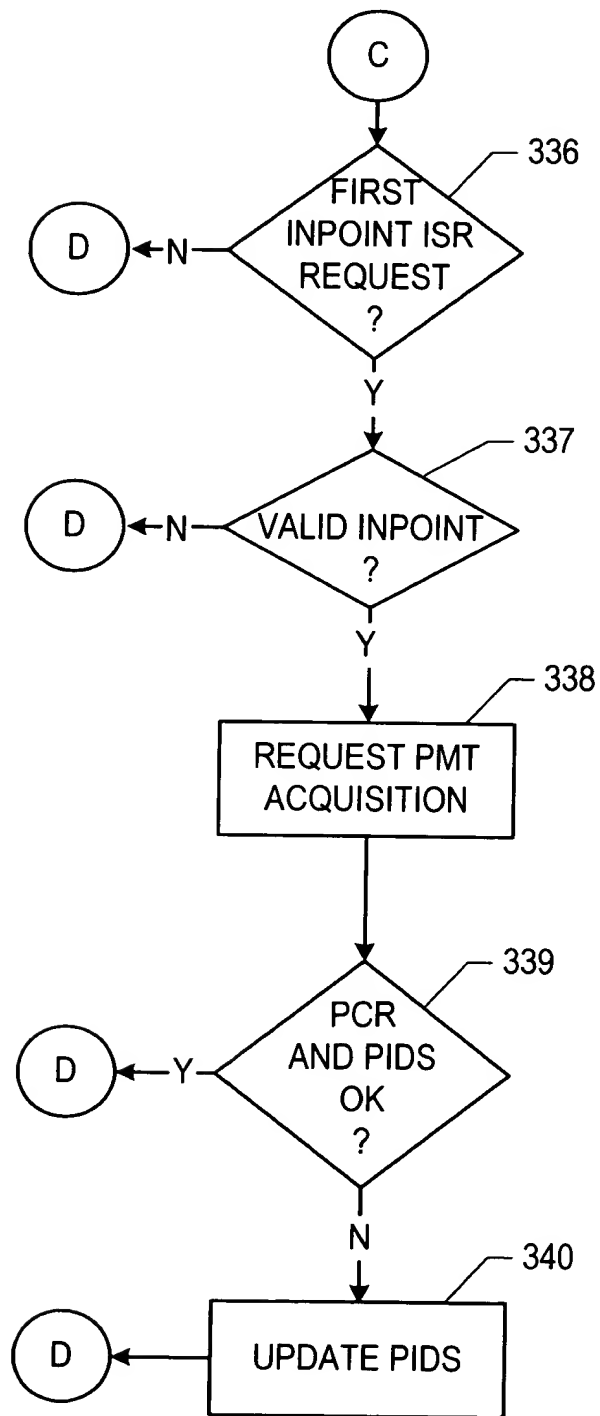


FIG. 37



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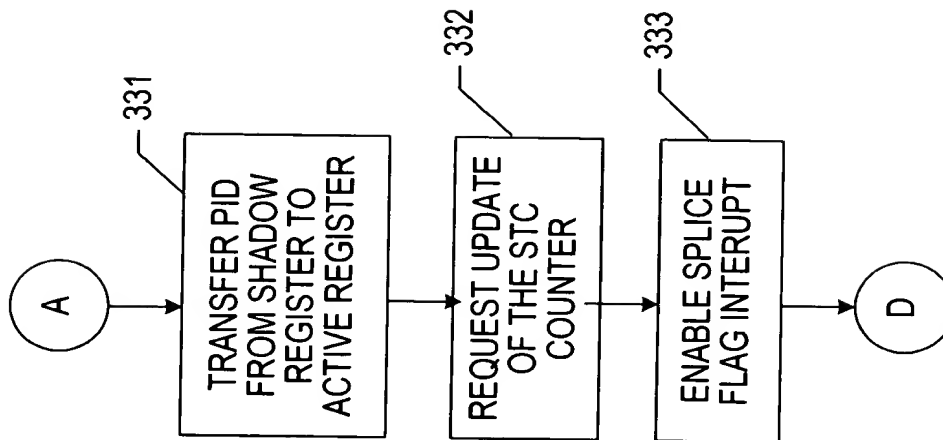


FIG. 38



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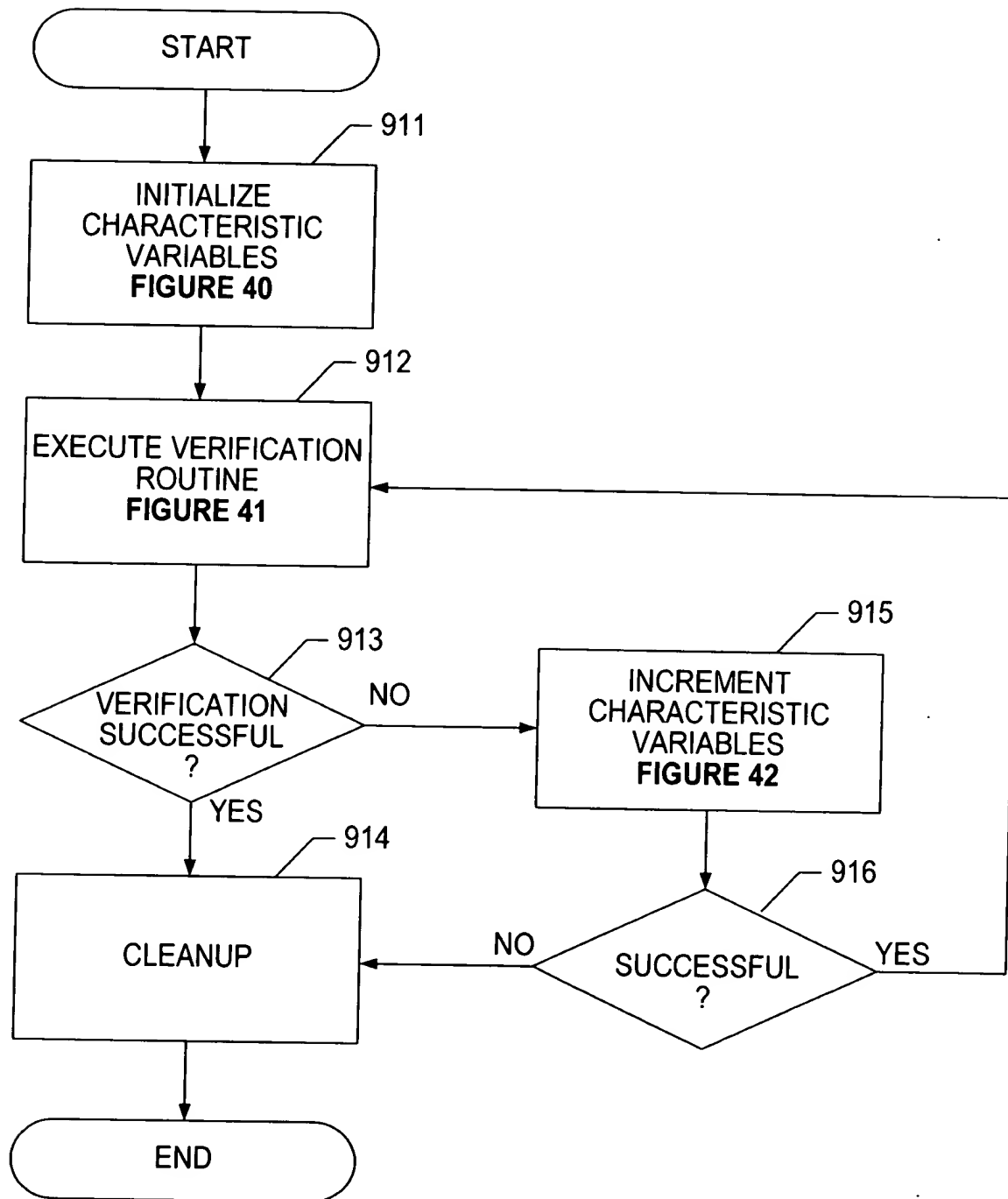


FIG. 39



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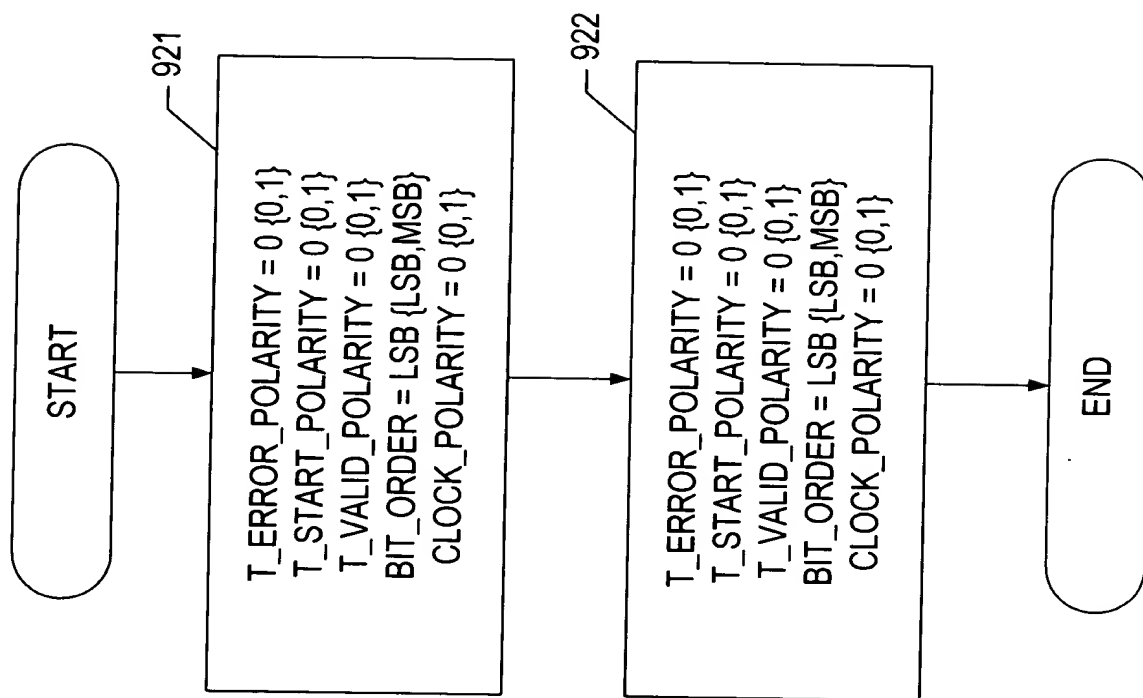


FIG. 40



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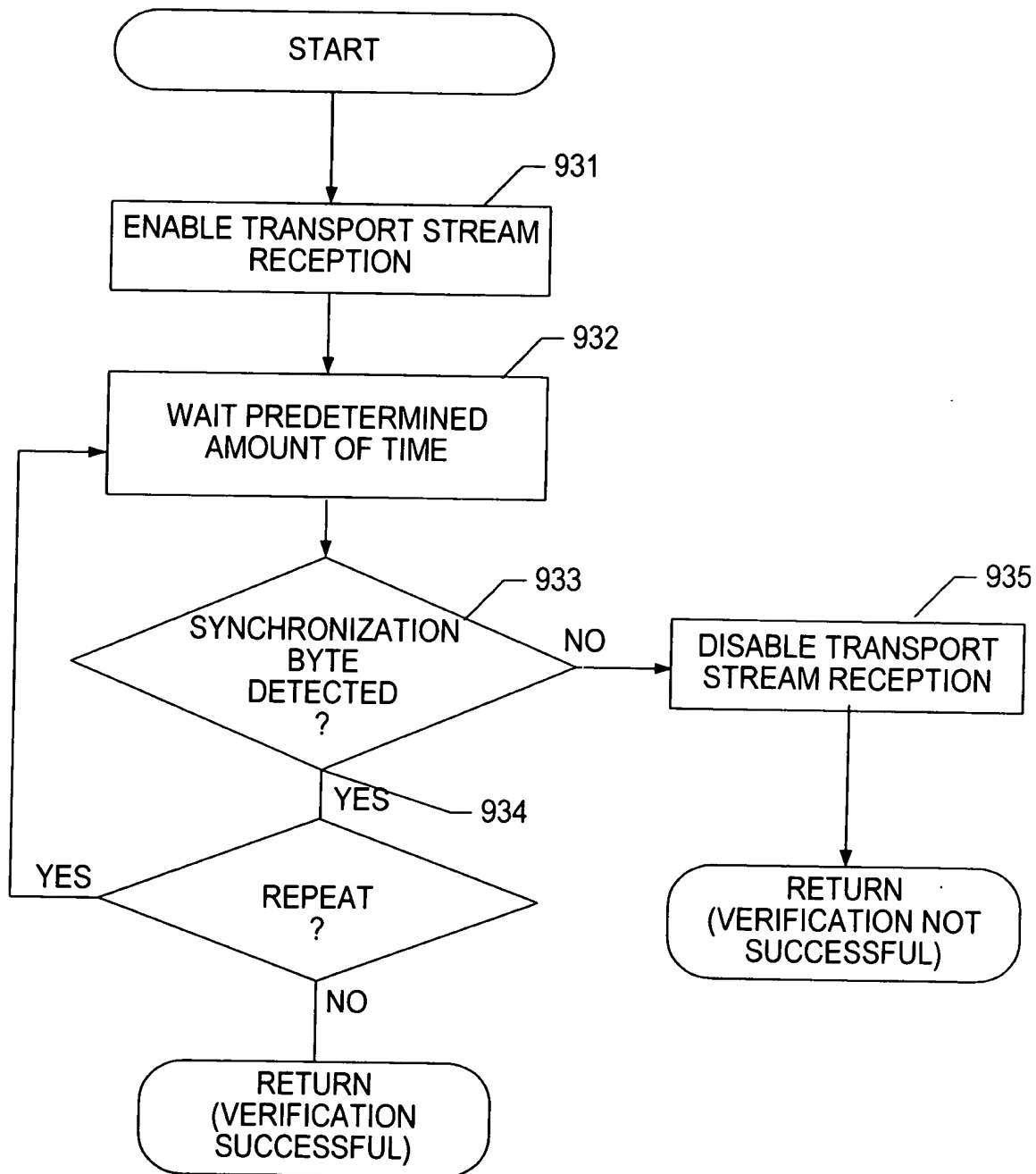
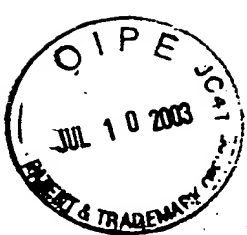


FIG. 41



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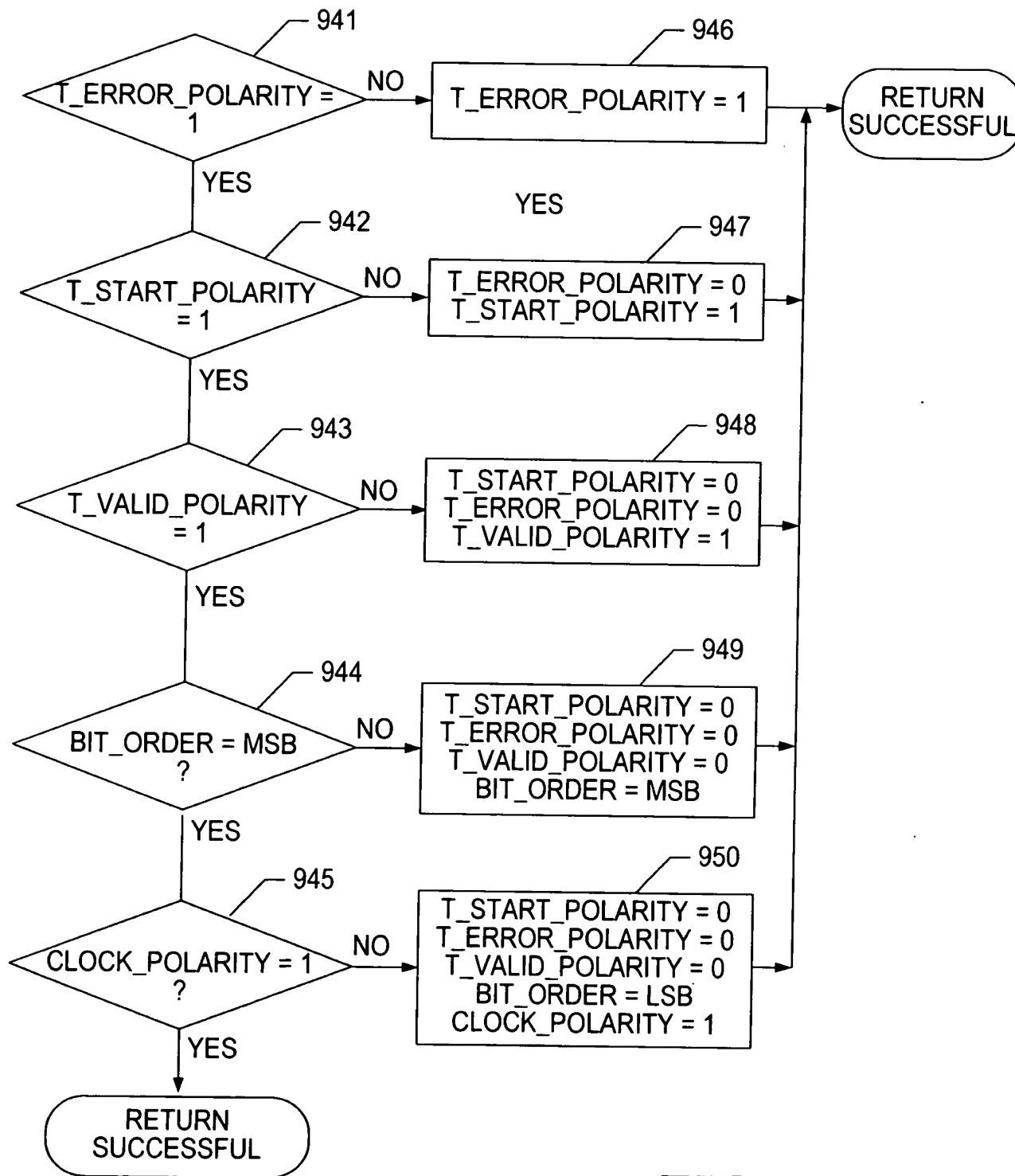


FIG. 42



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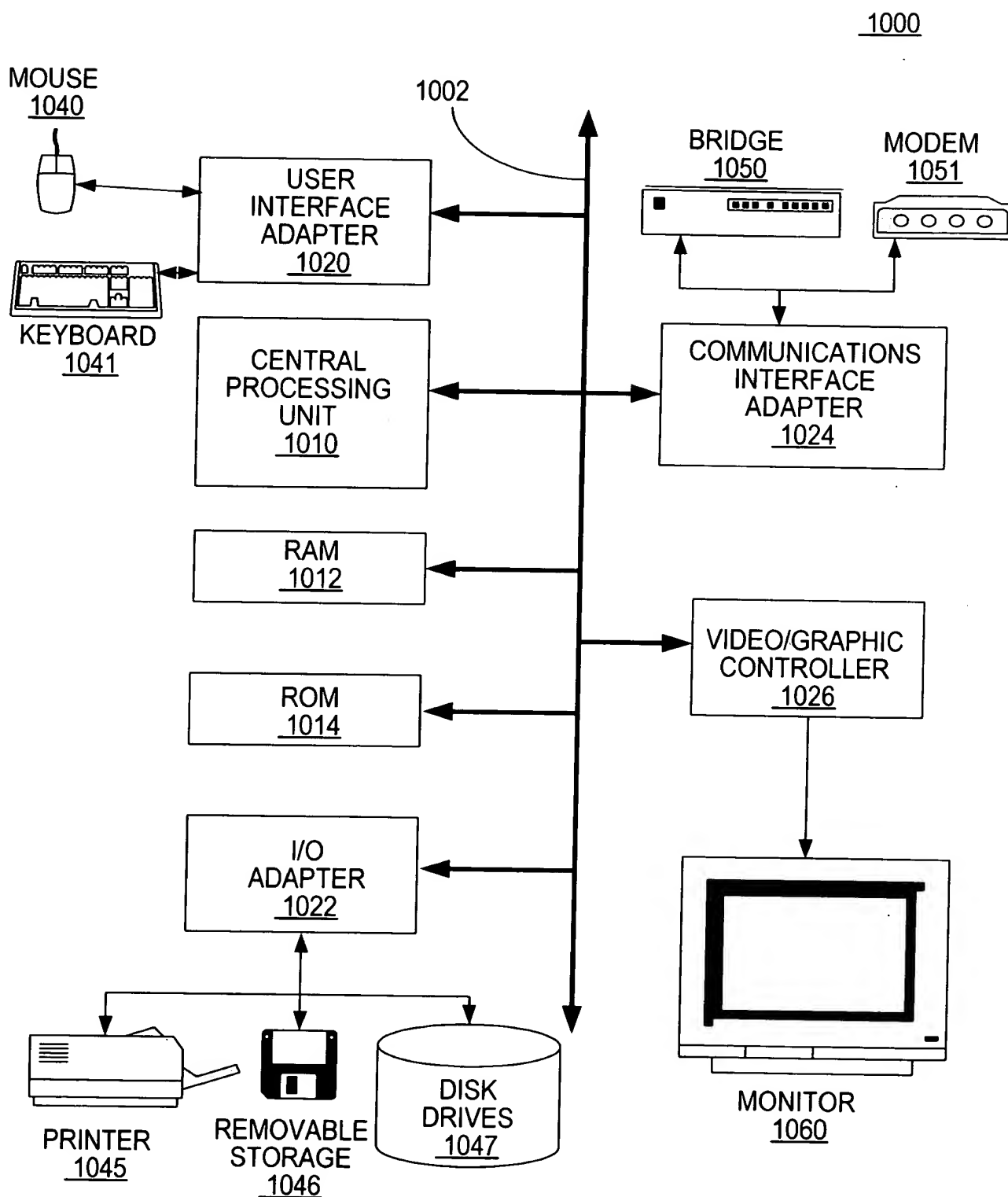


FIG. 43